NE RIEN ÉCRIRE DANS CE CADRE

MINISTÈRE DE L'ÉDUCATION NATIONALE

Académie : Session :

Concours :

Spécialité/option : Repère de l'épreuve :

Intitulé de l'épreuve :

NOM :
(en majuscules, suivi s'il y a lieu, du nom d'épouse)

Prénoms :

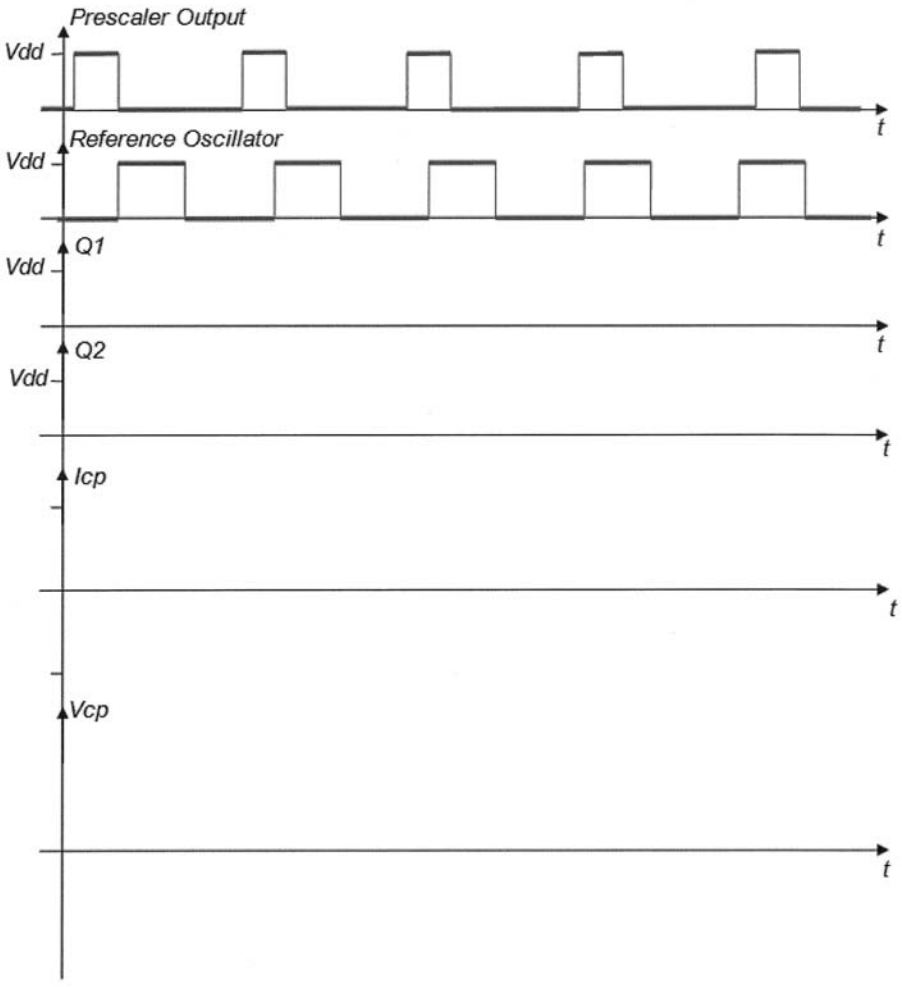
N° du candidat

(le numéro est celui qui figure sur la convocation ou la liste d'appel)

EAE GEE 2

C. Document réponse

DR1 : Caractérisation du fonctionnement du comparateur de phase (Q2.16)



C

RF2512

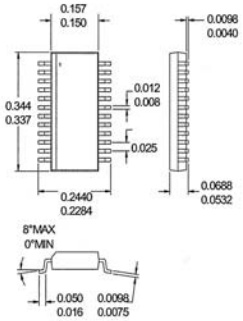
UHF TRANSMITTER

Typical Applications

- Single- or Dual-Channel LO Source
- FM/FSK Transmitter
- Wireless Data Transmitters
- 433/868/915MHz ISM Band Systems
- Wireless Security Systems

Product Description

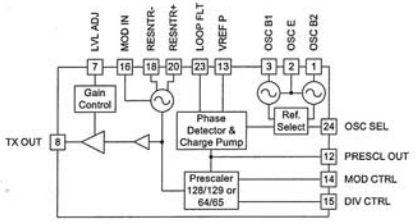
The RF2512 is a monolithic integrated circuit intended for use as a low-cost frequency synthesizer and transmitter. The device is provided in a 24 pin SSOP package and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in FM or FSK applications in the U.S. 915MHz ISM band and European 433MHz or 868MHz ISM band. The integrated VCO, dual-modulus/dual-divide (128/129 or 64/65) prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator. A second reference oscillator is available to support two channel applications.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- 15mW Output Power at 433MHz
- 2.7V to 5.0V Supply Voltage
- Low Current and Power Down Capability
- 300MHz to 1000MHz Frequency Range
- Narrowband and Wideband FM

Ordering Information

RF2512	UHF Transmitter
RF2512 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2512 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2512 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Tournez la page S.V.P.

D

D. Documentation

Absolute Maximum Ratings

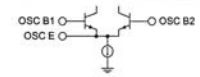
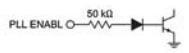
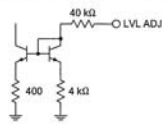
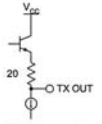
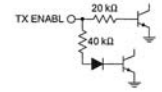
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

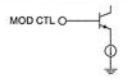
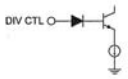
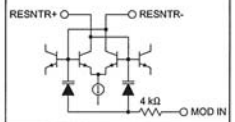
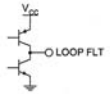
Caution! ESD sensitive device.

RF Micro Devices believes the furnished information is correct and accurate at the time of this printing. However, RF Micro Devices reserves the right to make changes to its products without notice. RF Micro Devices does not assume responsibility for the use of the described product(s).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		300 to 1000		MHz	
Modulation		FM/FSK			
Modulation Frequency			2	MHz	
Maximum FM Deviation	200			kHz	Dependent upon Supply Voltage
PLL and Prescaler					
Prescaler Divide Ratio		64/65 or 128/129			
PLL Lock TIme		4/PLL BW		ms	The PLL lock time, from power up, is set externally by the bandwidth of the loop filter.
PLL Phase Noise		-80		dBc/Hz	10kHz Offset, 10kHz loop bandwidth
		-100		dBc/Hz	100kHz Offset, 10kHz loop bandwidth
Reference Frequency			17	MHz	
Max Crystal R_S	TBD		100	Ω	
Charge Pump Current	-40		+40	µA	
Transmit Section					
Maximum Power Level	+7	+12		dBm	Freq=433MHz
		+6		dBm	Freq=915MHz
Power Control Range	15			dB	
Power Control Sensitivity		10		dB/V	
Antenna Port Impedance		50		Ω	TX ENABL="1"
Antenna Port VSWR			1.5:1		TX Mode
Modulation Input Impedance	4			kΩ	
Harmonics		-23		dBc	
Spurious				dBc	Compliant to Part 15.249 and I-ETS 300 220
Power Down Control					
Logic Controls "ON"	2.0			V	Voltage supplied to the input; device is "ON"
Logic Controls "OFF"			1.0	V	Voltage supplied to the input; device is "OFF"
Control Input Impedance	25			kΩ	
Turn On Time			5+4/PLL BW	ms	From Change in OSC SEL,7.075MHz XTAL
Turn Off Time			TBD	ms	From Change in OSC SEL,7.075MHz XTAL
Power Supply					
Voltage		3.6		V	Specifications
		2.7 to 5.0		V	Operating limits
Current Consumption		28		mA	TX Mode, LVL ADJ=3.6V
		10		mA	TX Mode, LVL ADJ=0V
		8		mA	PLL Only
			1	µA	LVL ADJ=0V, PLL ENABL=0V, TX ENABL=0V, OSC SEL=0V

RF2512

Pin	Function	Description	Interface Schematic
1	OSC B2	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 1 and pin 2.	
2	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. An appropriate capacitor as chosen by the customer should be connected from this pin to ground.	See pin 1.
3	OSC B1	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. An appropriate capacitor as chosen by the customer should be connected between pin 3 and pin 2.	See pin 1.
4	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL electronics. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
5	GND1	Ground connection for the PA buffer amp. Keep traces physically short and connect immediately to ground plane for best performance.	
6	VCC3	This pin is used to supply DC bias to the transmitter PA. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
7	LVL ADJ	This pin is used to vary the transmitter output power. An output level adjustment range greater than 12dB is provided through analog voltage control of this pin. DC current of the transmitter power amp ia also reduced with output power. This pin MUST be low when the transmitter is disabled.	
8	TX OUT	RF output pin for the transmitter electronics. TX OUT output impedance is a low impedance when the transmitter is enabled. TX OUT is a high impedance when the transmitter is disabled.	
9	GND2	Ground connection for the Tx PA functions. Keep traces physically short and connect immediately to ground plane for best performance.	
10	VCC1	This pin is used to supply DC bias to the PA buffer amp. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 100pF capacitor is recommended for 915MHz applications. A 220pF capacitor is recommended for 433MHz applications.	
11	TX ENABL	Enables the transmitter circuits. TX ENABL>2.0V powers up all transmitter functions. TX ENABL<1.0V turns off all transmitter functions except the PLL functions.	
12	PRESCL OUT	Dual-modulus/Dual-divide prescaler output. The output can be interfaced to an external PLL IC for additional flexibility in frequency programming.	
13	VREF P	Bias voltage reference pin for bypassing the prescaler and phase detector. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin.	

Pin	Function	Description	Interface Schematic
14	MOD CTRL	This pin is used to select the prescaler modulus. A logic "high" selects 64 or 128 for the prescaler divisor. A logic "low" selects 65 or 129 for the prescaler divisor.	
15	DIV CTRL	This pin is used to select the desired prescaler divisor. A logic "high" selects the 64/65 divisor. A logic low selects the 128/129 divisor.	
16	MOD IN	FM analog or digital modulation can be imparted to the VCO through this pin. The VCO varies in accordance to the voltage level presented to this pin. To set the deviation to a desired level, a voltage divider referenced to Vcc is the recommended. Because the modulation varactors are part of the resonator tank, the deviation is slightly dependent upon the components used in the external tank.	See pin 18.
17	VCC2	This pin is used to is supply DC bias to the VCO, prescaler, and PLL.	
18	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 20.	
19	NC	Not internally connected.	
20	RESNTR+	See pin 18.	See pin 18.
21	GND3	GND is the ground shared on chip by the VCO, prescaler, and PLL electronics. Keep traces physically short and connect immediately to ground plane for best performance.	
22	NC	Not internally connected.	
23	LOOP FLT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth.	
24	OSC SEL	A logic high (OSC SEL>2.0V) applied to this pin powers on reference oscillator 2 and powers down reference oscillator 1. A logic low (OSC SEL<1.0V) applied to this pin powers on reference oscillator 1 and powers down reference oscillator 2.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1-3, 9, 10, 12-15, 17, 21, 23.	

Tournez la page S.V.P.

RF2512 Theory of Operation

Introduction

The RF2512 is a low cost FM/FSK UHF transmitter designed for applications operating within the frequency range of 300MHz to 1000MHz. In particular, it is intended for 315/433/868MHz band systems, remote keyless entry systems, and FCC Part 15.231 periodic transmitters. It can also be used as a single- or dual-channel local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop.

The RF2512 is provided in a 24-pin SSOP-24 package and is designed to operate from a supply voltage ranging from 2.2V to 5.0V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to 15mW output power into a 50Ω load (+11.8dBm) and is intended to comply with FCC requirements for unlicensed remote control transmitters.

RF2512 Functional Blocks

A PLL consists of a reference oscillator, a phase detector, a loop filter, a voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2512 includes all of these internally except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillators** are Colpitts type oscillators. Pin 1 (OSC B2), pin 2 (OSC E), and pin 3 (OSC B1) provide connections to the internal transistors that are used as the reference oscillators. The Colpitts configuration is a low parts count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of either transistor. The drive level should, in either case, be around 500mV$_{PP}$. This level prevents overdriving the device and keeps the phase noise and reference spurs to a minimum.

The user sets which oscillator is operational by setting pin 24 (OSC SEL) either high or low. This allows the implementation of two channel systems.

The **prescaler** divides the Voltage Controlled Oscillator (VCO) frequency down by either 64/65 or 128/129, using a series of flip-flops, depending upon the logic level present at pin 15 (DIV CTRL). A high logic level will select the 64/65 divisor. A low logic level will select the 128/129 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

In addition to the DIV CTRL setting, one also sets the prescaler modulus by setting pin 14 (MOD CTRL) either high or low. A high logic level will select the 64/128 divisor. A low logic level will select the 65/129 divisor.

Pin 12 (PRESCL OUT) provides access to the prescaler output. This is used for interfacing to an external PLL IC.

The RF2512 contains an onboard phase detector and charge pump. The **phase detector** compares the phase of the reference oscillator to the phase of the VCO. The phase detector is implemented using flip-flops in a topology referred to as either "digital phase/frequency detector" or "digital tri-state comparator". The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency.

When both inputs of the flip-flops are identical, the signals are both frequency and phase locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter or enter into a high impedance state. This is where the name "tri-state comparator" comes from.

The main benefit of this type of detector it's ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it will use the frequency error for correction. This type of detector will lock under all conditions.

The prescaler and the phase detector bias voltage is brought out through pin 13 (VREF P). This allows bypassing of the of these two circuits to filter the reference crystal frequency.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. It's inputs are the outputs of the phase detector flip-flops. Since there are two flip-flops, there are four possible states. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. The

state where both inputs are high will not occur. The other states are either charging or discharging the loop filter. The loop filter integrates the pulses coming from the charge pump to create a control voltage for the voltage controlled oscillator.

The **voltage controlled oscillator** (VCO) is a tuned differential amplifier with the bases and collectors cross coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors. It is comprised an external varactor, a capacitor and external inductors. The designer selects the inductors for the desired frequency of operation. These inductors also provide DC bias for the VCO. The output of the VCO is buffered and applied to the prescaler circuit, where it is divided down and compared to the reference oscillator frequency.

The PLL and VCO circuitry can be enabled by setting applying a "high" logic level to pin 4 (PLL ENABL). Conversely, the PLL and VCO circuitry will be turned off if the level is tied "low".

The **transmit amplifier** is a two stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 12dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The output power is adjustable by the setting of pin 7 (LVL ADJ). This analog input allows the designer a 12dB range of output power. As the LVL ADJ voltage is reduced, the output power and current consumption are reduced. LVL ADJ must be low when the transmitter is disabled.

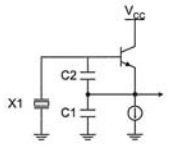
Additionally, the transmitter circuitry can be disabled entirely by applying a "low" logic level to pin 11 (TX ENABL). During transmission, this pin should be tied "high". This pin controls all circuitry except for the PLL circuitry.

During transmission the transmitter is enabled and the impedance of the output pin, pin 8 (TX OUT), is low. When the transmitter is not enabled, the impedance becomes high.

The RF2512 contains onboard band gap reference voltage circuitry which provides a stable **DC bias** over varying temperature and supply voltages.

Designing with the RF2512

The **reference oscillator** is built around the onboard transistor at pins 1, 2 and 3. The intended topology is of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low cost solutions. The topology of this type of oscillator is as seen in the following figure.



This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C1 and C2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations.

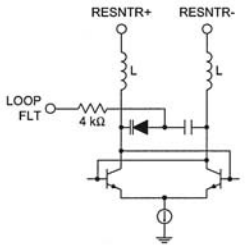
$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

The load capacitance is usually 32pF. The variable *freq* is the oscillator frequency in MHz. The frequency can be adjusted by either changing C_2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at pin 2 (OSC E). It has been found that the level at this pin should generally be around 500mV$_{PP}$ or less. This will reduce the reference spur levels and reduce noise from distortion. If this level is higher than 500mV$_{PP}$ then decrease the value of C_1. The values of these capacitors are usually tweaked during design to meet performance goals, such as minimizing the start-up time.

Additionally, by placing a variable capacitor in series with the crystal, one is able to adjust the frequency. This will also alter the drive level, so it should be checked again.

An important part of the overall design is the **voltage controlled oscillator**. The VCO is configured as a differential amplifier. The VCO is tuned via the external inductors, capacitor, and varactor. The varactor capacitance is set by the loop filter output voltage through a 4kΩ resistor.



To tune the VCO the designer only needs to calculate the value of the inductors connected to pins 18 and 20 (RESNTR- and RESNTR+). The inductor value is determined by the following equation.

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C} \cdot \frac{1}{2}$$

In this equation, *f* is the desired operating frequency and *L* is the value of the inductor required. The value *C* is the amount of capacitance presented by the varactor, capacitor and parasitics. The factor of one-half is due to the inductors being in each leg.

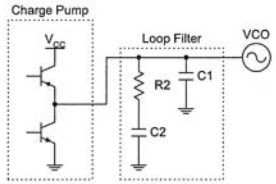
The setup of the VCO can be summarized as follows. First, open the loop. Next, get the VCO to run on the desired frequency by selecting the proper inductor and capacitor values. The capacitor value will need to include the varactor and circuit parasitics. After the VCO is running at the desired frequency, then set the VCO sensitivity.

The sensitivity is determined by connecting the control voltage input point to ground and noting the frequency. Then connect the same point to the supply and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sensitivity expressed in Hz/V. Increasing the inductor value while decreasing the capacitor value will increase the sensitivity. Decreasing the inductor value while increasing the capacitor value will lower the sensitivity.

When increasing or decreasing component values, make sure that the center frequency remains constant. Finally, close the loop.

External to the part, the designer needs to implement a **loop filter** to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through a 4kΩ resistor. The loop filter is then connected in parallel to this point at pin 23 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC. A passive filter is most common, as it is a low cost and low noise design. An additional pole could be used for reducing the reference spurs, however there is not a way to add the series resistor. This should not be a reason for concern however.

The schematic of the loop filter is



RF2512

11
TRANSCEIVERS

The control lines provide an **interface** for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 16 (MOD IN), pin 15 (DIV CTRL), pin 14 (MOD CTRL) and pin 7 (LVL ADJ) as control pins whose voltage level can be set.

General **RF bypassing** techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias for connection to the ground plane allows one to connect to ground as close as possible to ground pins. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

Pre-compliance testing should be performed during the design process. This can be done with a GTEM cell or at a compliance testing laboratory. It is recommended that pre-compliance testing be performed so that there are no surprises during final compliance testing. This will help keep the product development and release on schedule.

Working with a laboratory offers the benefit of years of compliance testing experience and familiarity with the regulatory issues. Also, the laboratory can often provide feedback that will help the designer make the product compliant.

On the other hand, having a GTEM cell or an open air test site locally offers the designer the ability to rapidly determine whether or not design changes impact the product's compliance. Set-up of an open air test site and the associated calibration is not trivial. An alternative is to use a GTEM test cell.

After the design has been completed and passes compliance testing, application will need to be made with the respective regulatory bodies for the geographic region in which the product will be operated to obtain final certifications.

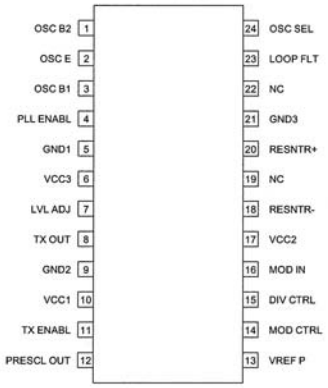
Conclusions

The RF2512 is an FM/FSK UHF transmitter that features a phase-locked output. This device is suitable for use in a CFR Part 15.231 compliant product as well as a local oscillator signal source. Further, the RF2512 is packaged in a low cost SSOP-24 plastic package and requires few external parts, thus making it suitable for low cost designs.

Tournez la page S.V.P.

RF2512

Pin Out

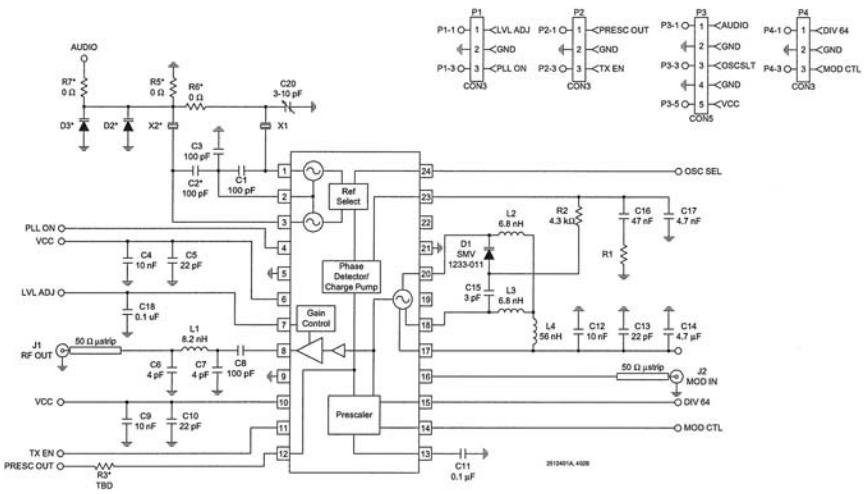


11
TRANSCEIVERS

Rev B9 010509

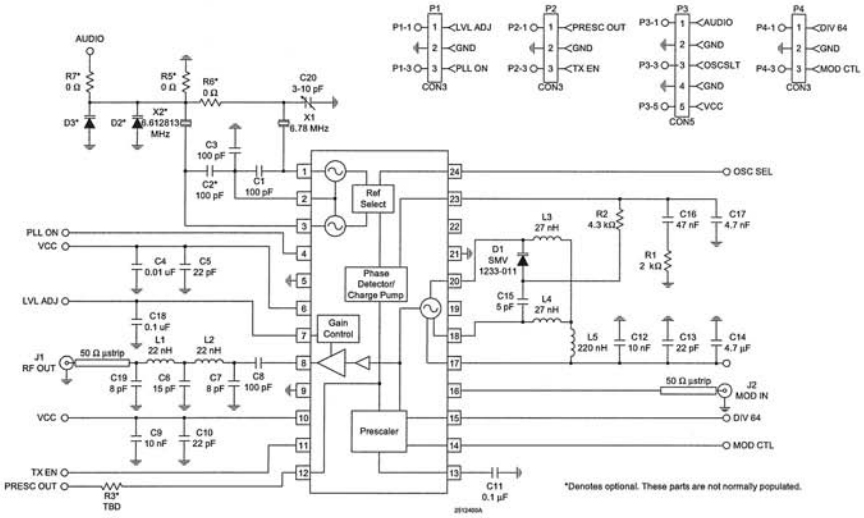
Evaluation Board Schematic
H (915MHz) and M (868MHz) Boards

(Download Bill of Materials from www.rfmd.com.)



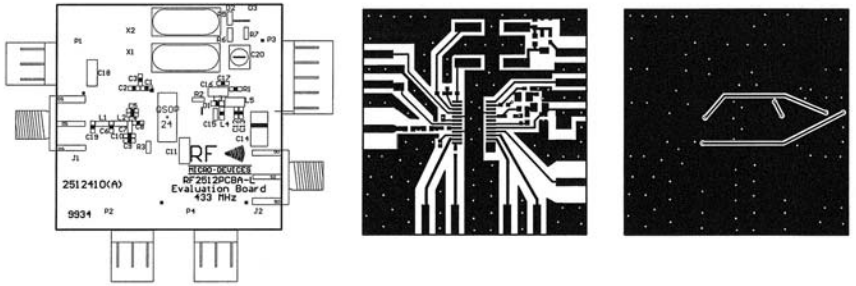
Board	X1 (MHz)	X2 (MHz)	R1 (kΩ)	L2 (nH)	L3 (nH)
M (868MHz)	13.57734	13.41015	1.2	6.8	6.8
H (915MHz)	7.15909	7.07549	2.2	4.7	4.7

Evaluation Board Schematic
L (433MHz) Board

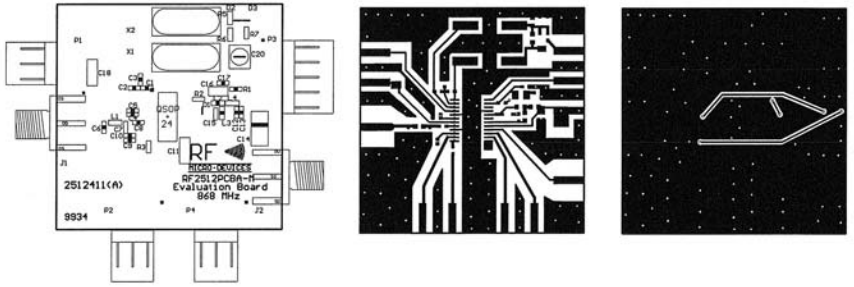


*Denotes optional. These parts are not normally populated.

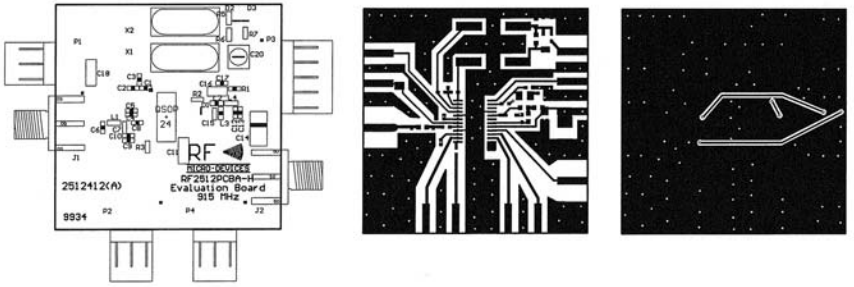
Evaluation Board Layout 433MHz
Board Size 1.5" x 1.5"



Evaluation Board Layout 868MHz
Board Size 1.5" x 1.5"

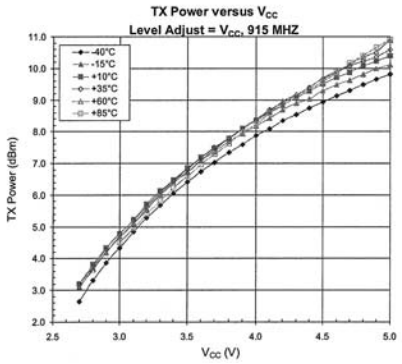


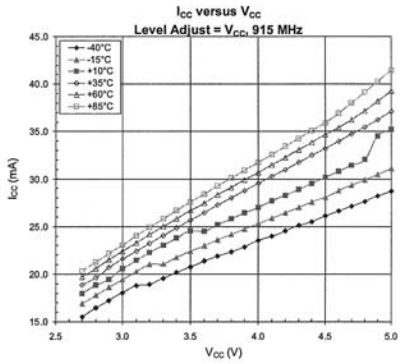
Evaluation Board Layout 915MHz
Board Size 1.5" x 1.5"



11
TRANSCEIVERS

Tournez la page S.V.P.





11
TRANSCEIVERS

SKYWORKS®

DATA SHEET

SMV1231–SMV1237: Hyperabrupt Tuning Varactors

Features

- High capacitance ratio
- Low series resistance for low phase noise
- Multiple packages SOT-23, SOD-323, SC-70 and SC-79
- Designed for high-volume commercial applications
- Full characterization with SPICE models
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

Description

The SMV1231–SMV1237 series of silicon hyperabrupt junction varactor diodes is designed for use in VCOs with low tuning voltage operation. The low resistance of these varactors makes them appropriate for high Q resonators in wireless system VCOs to frequencies beyond 2.5 GHz. The SMV1231–SMV1237 series is fully characterized for capacitance and resistance over temperature. SPICE model is provided.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Absolute Maximum Ratings

Characteristic	Value
Reverse voltage (V_R)	15 V
Forward current (I_F)	20 mA
Power dissipation (P_D)	250 mW
Storage temperature (T_{ST})	-55 °C to +150 °C
Operating temperature (T_{OP})	-55 °C to +125 °C
ESD human body model	Class 1B

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

					
Single	Single	Single	Common Cathode	Common Anode	Common Cathode
SC-79	SOD-323	SOT-23	SOT-23	SC-70	SC-70
SMV1231-079 Marking: Cathode	**SMV1231-011** Marking: JA				**SMV1231-074** Marking: JA3
SMV1231-079LF Marking: Cathode	**SMV1231-011LF** Marking: KA				**SMV1231-074LF** Marking: KA3
SMV1232-079 Marking: Cathode	**SMV1232-011** Marking: CC				**SMV1232-074** Marking: CC3
SMV1232-079LF Marking: Cathode	**SMV1232-011LF** Marking: HC				**SMV1232-074LF** Marking: HC3
SMV1233-079 Marking: Cathode	**♦SMV1233-011** Marking: VP	**SMV1233-001** Marking: VP1	**SMV1233-004** Marking: VP3		**SMV1233-074** Marking: VP3
SMV1233-079LF Marking: Cathode	**♦SMV1233-011LF** Marking: DP	**SMV1233-001LF** Marking: DP1	**SMV1233-004LF** Marking: DP3		**SMV1233-074LF** Marking: DP3
SMV1234-079 Marking: Cathode	**♦SMV1234-011** Marking: VQ	**SMV1234-001** Marking: VQ1	**SMV1234-004** Marking: VQ3	**SMV1234-073** Marking: VQ9	
SMV1234-079LF Marking: Cathode	**♦SMV1234-011LF** Marking: DQ	**SMV1234-001LF** Marking: DQ1	**SMV1234-004LF** Marking: DQ3	**SMV1234-073LF** Marking: DQ9	
SMV1235-079 Marking: Cathode	**SMV1235-011** Marking: VR	**SMV1235-001** Marking: VR1	**SMV1235-004** Marking: VR3		**SMV1235-074** Marking: VR3
SMV1235-079LF Marking: Cathode	**SMV1235-011LF** Marking: DR	**SMV1235-001LF** Marking: DR1	**SMV1235-004LF** Marking: DR3		**SMV1235-074LF** Marking: DR3
♦SMV1236-079 Marking: Cathode	**SMV1236-011** Marking: AQ	**SMV1236-001** Marking: AQ1	**SMV1236-004** Marking: AQ3		**SMV1236-074** Marking: AQ3
♦SMV1236-079LF Marking: Cathode	**SMV1236-011LF** Marking: EQ	**SMV1236-001LF** Marking: EQ1	**SMV1236-004LF** Marking: EQ3		**SMV1236-074LF** Marking: EQ3
		SMV1237-001 Marking: VT1			
		SMV1237-001LF Marking: DT1			
L_S = 0.7 nH	L_S = 1.5 nH	L_S = 1.5 nH	L_S = 1.5 nH	L_S = 1.4 nH	L_S = 1.4 nH

LF denotes lead (Pb)-free, RoHS-compliant packaging option as an alternative to our standard tin/lead (Sn/Pb) packaging.

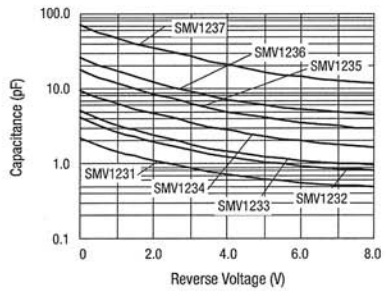
Innovation to Go™
Select Linear Products (indicated by ♦) now available for purchase online.

Electrical Specifications at 25 °C

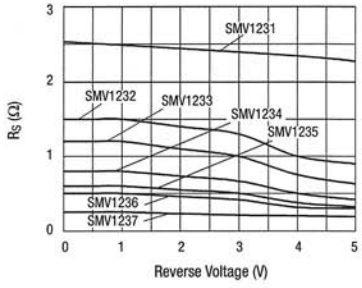
Part Number	C_T @ 1 V (pF)		C_T @ 3 V (pF)	C_T @ 6 V (pF)	$\frac{C_T @ 1 V}{C_T @ 3 V}$ (Ratio)		$\frac{C_T @ 1 V}{C_T @ 6 V}$ (Ratio)		R_S @ 3 V 500 MHz (Ω)	Q @ 3 V 50 MHz
	Min.	Max.	Typ.	Typ.	Min.	Max.	Min.	Max.	Max.	Typ.
SMV1231	1.43	1.72	0.97	0.61	1.5	1.8	2.5	2.8	2.9	1500
SMV1232	2.34	2.86	1.5	0.94	1.5	1.9	2.6	3.3	1.5	1400
SMV1233	3	3.6	1.8	1.1	1.5	1.9	2.6	3.3	1.2	1200
SMV1234	5.85	7.15	3.6	2	1.6	2	2.8	3.4	0.8	1000
SMV1235	10.35	12.65	6.4	3.6	1.6	2	2.9	3.4	0.6	750
SMV1236	15.5	18.5	9.2	5.3	1.6	2	3	3.5	0.5	700
SMV1237	45	54	26.9	14.4	1.6	2	3	3.5	0.25	500

Tested in -079 package.
Reverse Voltage V_R (I_R = 10 µA): 15 V minimum.
Reverse Current I_R (V_R = 12 V): 20 nA maximum.

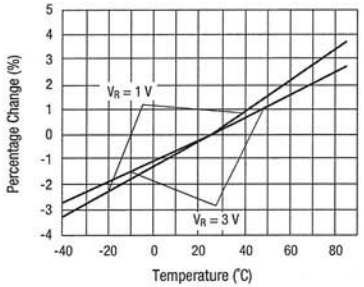
Typical Performance Data



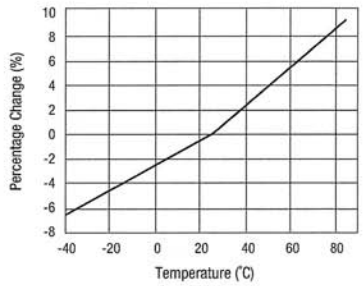
Capacitance vs. Reverse Voltage



Series Resistance vs. Reverse Voltage @ 500 MHz



Relative Capacitance Change vs. Temperature

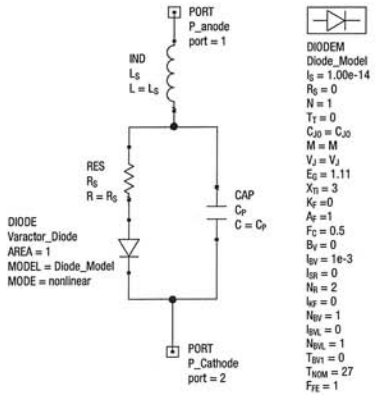


Relative Series Resistance Change vs. Temperature @ 500 MHz

Typical Capacitance Values

V_R (V)	SMV1231 C_T (pF)	SMV1232 C_T (pF)	SMV1233 C_T (pF)	SMV1234 C_T (pF)	SMV1235 C_T (pF)	SMV1236 C_T (pF)	SMV1237 C_T (pF)
0	2.35	4.15	5.08	9.63	18.22	26.75	71.82
0.5	1.87	3.22	3.95	7.53	14.12	20.61	56.1
1	1.58	2.67	3.28	6.28	11.67	17.02	46.89
1.5	1.4	2.28	2.8	5.39	9.91	14.38	40.33
2	1.22	1.97	2.41	4.68	8.52	12.29	35.13
2.5	1.09	1.72	2.09	4.09	7.36	10.56	30.71
3	0.97	1.51	1.82	3.58	6.4	9.16	26.87
3.5	0.882	1.35	1.62	3.15	5.62	8.04	23.57
4	0.794	1.22	1.45	2.81	4.99	7.19	20.83
4.5	0.732	1.13	1.33	2.54	4.5	6.53	18.62
5	0.683	1.05	1.24	2.32	4.11	6.01	16.87
5.5	0.648	0.99	1.16	2.15	3.8	5.61	15.48
6	0.613	0.94	1.1	2.02	3.55	5.28	14.36
6.5	0.59	0.9	1.05	1.9	3.34	5.02	13.46
7	0.567	0.86	1.01	1.8	3.17	4.81	12.72
7.5	0.551	0.84	0.98	1.72	3.03	4.64	12.11
8	0.534	0.81	0.96	1.65	2.91	4.49	11.61
9	0.512	0.78	0.92	1.55	2.73	4.28	10.87
10	0.497	0.76	0.9	1.47	2.61	4.13	10.38
11	0.492	0.75	0.88	1.42	2.53	4.02	10.06
12	0.487	0.74	0.87	1.38	2.47	3.95	9.84
13	0.48	0.73	0.86	1.35	2.43	3.89	9.68
14	0.472	0.73	0.85	1.33	2.4	3.84	9.56
15	0.466	0.72	0.84	1.32	2.38	3.8	9.47

SPICE Model



Part Number	C_{J0} (pF)	V_J (V)	M	C_P (pF)	R_S (Ω)
SMV1231	–	1.5	0.8	0	2.5
SMV1232	4.2	1.7	0.9	0	1.5
SMV1233	4.12	1.7	0.9	0.7	1.2
SMV1234	8.75	2.3	1.1	1.2	0.8
SMV1235	16.13	8	4	2	0.6
SMV1236	21.63	8	4.2	3.2	0.5
SMV1237	66.16	10	5.3	9	0.25

Values extracted from measured performance.
For package inductance (L_S) refer to package type.
For more details refer to the "Varactor SPICE Models for RF VCO Applications" Application Note.

Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

Tournez la page S.V.P.

RF2917

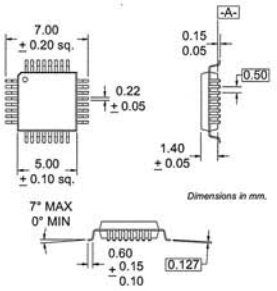
433/868/915MHZ FM/FSK RECEIVER

Typical Applications

- Wireless Meter Reading
- Keyless Entry Systems
- 433/868/915MHz ISM Band Systems
- Remote Data Transfers
- Wireless Security Systems

Product Description

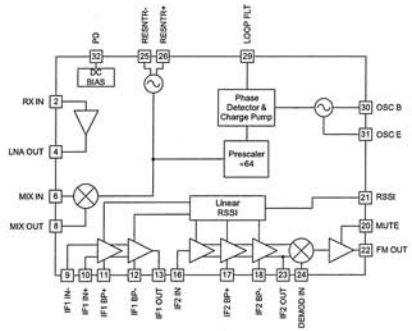
The RF2917 is a monolithic integrated circuit intended for use as a low cost FM or FSK receiver. The device is provided in 32-lead plastic packaging and is designed to provide a fully functional FM receiver. The chip is intended for analog or digital applications in the North American 915MHz ISM band and European 433MHz and 868MHz ISM bands. The integrated VCO, ÷64 prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked oscillator for single channel applications. The selection of linear FM output or digital FSK output is done with the mute pin.



Package Style: LQFP-32_5x5

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Fully Monolithic Integrated Receiver
- 2.7V to 5.0V Supply Voltage
- Narrowband and Wideband FSK
- 300MHz to 1000MHz Frequency Range
- Power Down Capability
- Analog or Digital Output

Ordering Information

RF2917	433/868/915MHz FM/FSK Receiver
RF2917 PCBA-L	Fully Assembled Evaluation Board, 433MHz
RF2917 PCBA-M	Fully Assembled Evaluation Board, 868MHz
RF2917 PCBA-H	Fully Assembled Evaluation Board, 915MHz

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

11 TRANSCEIVERS

11 TRANSCEIVERS

RF2917

Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +5.5	V_{DC}
Control Voltages	-0.5 to +5.0	V_{DC}
Input RF Level	+10	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

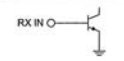
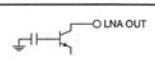
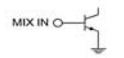
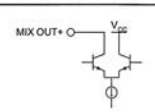
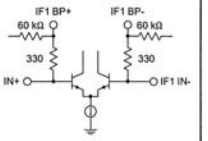
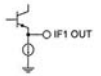
Caution! ESD sensitive device.

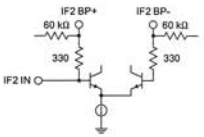
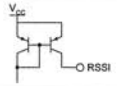
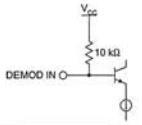
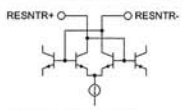
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25 °C, V_{CC}=3.6V, Freq=915MHz
RF Frequency Range		300 to 1000		MHz	
VCO and PLL Section					
VCO Frequency Range		300 to 1000		MHz	
PLL Lock Time		10		ms	The PLL lock time is set externally by the bandwidth of the loop filter and start up of the crystal.
PLL Phase Noise		-74		dBc/Hz	915MHz, 5kHz loop BW, 10kHz offset
		-98		dBc/Hz	915MHz, 5kHz loop BW, 100kHz offset
Reference Frequency	0.5		17	MHz	
Crystal R_S		50	100	Ω	
Charge Pump Current	-40		+40	µA	
Overall Receive Section					
Frequency Range		300 to 1000		MHz	
RX Sensitivity	-98	-101		dBm	IF BW=180kHz, Freq=915MHz, S/N=8dB
LO Leakage		-55		dBm	
RSSI DC Output Range		0.8 to 1.5		V	MUTE = 0; R_L = 51kΩ
RSSI Sensitivity		13		mV/dB	MUTE = 0
RSSI Dynamic Range		60		dB	MUTE = 0
LNA					
Power Gain		18		dB	433MHz, Matched to 50Ω
		16		dB	915MHz, Matched to 50Ω
Noise Figure		3.6		dB	433MHz
		3.8		dB	915MHz
Input IP_3		-8		dBm	915MHz
Input P_{1dB}		-15		dBm	915MHz
RX IN Impedance		82-j86		Ω	433MHz (see Plots)
		77-j43			915MHz (see Plots)
Output Impedance		Open Collector		Ω	
Mixer					Single-ended configuration
Conversion Power Gain		15		dB	433MHz, Matched to 50Ω
		8		dB	915MHz, Matched to 50Ω
Noise Figure (SSB)		17		dB	433MHz, SSB Measurement
		17		dB	915MHz, SSB Measurement
Input IP_3		-20		dBm	433MHz
Input IP_3		-15.5		dBm	915MHz
Input P_{1dB}		-30		dBm	433MHz
Input P_{1dB}		-26		dBm	915MHz
First IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		34		dB	IF=10.7MHz, Z_L=330Ω
Noise Figure		13		dB	
IF1 Input Impedance		330		Ω	
IF1 Output Impedance		330		Ω	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Second IF Section					
IF Frequency Range	0.1	10.7	25	MHz	
Voltage Gain		60		dB	IF=10.7MHz
Noise Figure		13		dB	
IF2 Input Impedance		330		Ω	
IF2 Output Impedance		1		kΩ	At IF2 OUT- pin 23
Demod Input Impedance		10		kΩ	Pin 24
Data Output Impedance		6.3 - j25.7		kΩ	
Data Output Bandwidth		500		kHz	Z_{LOAD}=1MΩ || 3pF; 3dB dependent on IF and discriminator BW
Data Output Level	0.3		V_{CC}-0.3	V	Z_{LOAD}=1MΩ || 3pF; Output voltage is proportional with the instantaneous frequency deviation.
FM Output DC Level		2.6		V	
FM Output AC Level		200		mV_{PP}	
Power Down Control					
Logical Controls "ON"	2.0			V	Voltage supplied to the input
Logical Controls "OFF"			1.0	V	Voltage supplied to the input
Control Input Impedance	25			kΩ	
Turn On Time		10.2		ms	From PD=1 to valid data out, current eval board
Power Supply					
Voltage		3.6		V	Specifications
	2.7		5.0	V	Operating limits
	2.4			V	Temp>0°C
Current Consumption	5	9	12.3	mA	RX Mode, MUTE="1"
			1	μA	Power Down Mode

Tournez la page S.V.P.

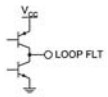
RF2917

Pin	Function	Description	Interface Schematic
1	VCC1	This pin is used to supply DC bias to the receiver RF electronics. A RF bypass capacitor should be connected directly to this pin and returned to ground. A 22pF capacitor is recommended for 915MHz applications. A 100pF capacitor is recommended for 433MHz applications.	
2	RX IN	RF input pin for the receiver electronics. RX IN input impedance is a low impedance when enabled. RX IN is a high impedance when the receiver is disabled.	
3	GND1	Ground connection for RF receiver functions. Keep traces physically short and connect immediately to ground plane for best performance.	
4	LNA OUT	Output pin for the receiver RF low noise amplifier. This pin is an open collector output and requires an external pull up coil to provide bias and tune the LNA output. A capacitor in series with this output can be used to match the LNA to 50Ω impedance image filters.	
5	GND2	GND2 is connection for the 40 dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
6	MIX IN	RF input to the RF Mixer. An LC matching network between LNA OUT and MIX IN can be used to connect the LNA output to the RF mixer input in applications where an image filter is not needed or desired.	
7	GND3	GND3 is the ground connection for the receiver RF mixer.	
8	MIX OUT	IF output from the RF mixer. Interfaces directly to 10.7MHz ceramic IF filters as shown in the application schematic. A pull-up inductor and series matching capacitor should be used to present a 330Ω termination impedance to the ceramic filter. Alternately, an IF tank can be used to tailor the IF frequency and bandwidth to meet the needs of a given application. In addition to the matching components, a 15pF capacitor should be placed from this pin to ground.	
9	IF1 IN-	Balanced IF input to the 40dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input.	
10	IF1 IN+	Functionally the same as pin 9 except non-inverting node amplifier input. In single-ended applications, this input should be bypassed directly to ground through a 10nF capacitor.	See pin 9.
11	IF1 BP+	DC feedback node for the 40dB limiting amplifier strip. A 100nF bypass capacitor from this pin to ground is required.	See pin 9.
12	IF2 BP-	See pin 11.	See pin 9.
13	IF1 OUT	IF output from the 40dB limiting amplifier. The IF1 OUT output presents a nominal 330Ω output resistance and interfaces directly to 10.7MHz ceramic filters.	
14	VREF IF	DC voltage reference for the IF limiting amplifiers (typically 1.1V). A 0.1μF capacitor from this pin to ground is required.	
15	GND5	Ground connection for 60dB IF limiting amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	

Pin	Function	Description	Interface Schematic
16	IF2 IN	Inverting input to the 60dB limiting amplifier strip. A 10nF DC blocking capacitor is required on this input. The IF2 IN input presents a nominal 330Ω input resistance and interfaces directly to 10.7MHz ceramic filters.	
17	IF2 BP+	DC feedback node for the 60dB limiting amplifier strip. A 100nF bypass capacitor from this pin to ground is required.	See pin 16.
18	IF2 BP-	See pin 17.	See pin 16.
19	VCC3	This pin is used to supply DC bias to the 60dB IF limiting amplifier. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
20	MUTE	This pin is used to select FM, FSK, or mute at the FM OUT pin. MUTE>Vcc - 0.4V turns the FM OUT signal off. MUTE<0.4V turns the FM OUT signal on for FSK digital data. When MUTE is left floating, the FM OUT signal is linear FM.	
21	RSSI	A DC voltage proportional to the received signal strength is output from this pin. The output voltage increases with increasing signal strength.	
22	FM OUT	Demodulated output from the discriminator/demodulator. Output levels on this are CMOS compatible in FSK mode (see pin 20). In linear FM mode, the demodulated signal level is approximately 240mVpp on a DC voltage offset. The magnitude of the load impedance is intended to be 1MΩ or greater.	
23	IF2 OUT	IF output from the 60dB limiting amplifier strip. This pin is intended to be connected to pin 24 through a 5pF capacitor (for 10.7MHz IF applications). This capacitor in conjunction with a tank resonant at the IF frequency connected from pin 24 to ground is used to form an FM discriminator.	
24	DEMOD IN	This pin is the input to the FM demodulator. This pin is NOT AC coupled. Therefore, a DC blocking capacitor is required on this pin to avoid a DC path to ground. A DC blocked LC tank resonant at the IF or ceramic discriminator should be connected to this pin.	
25	RESNTR-	This port is used to supply DC voltage to the VCO as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 26.	
26	RESNTR+	See pin 25.	See pin 25.
27	VCC2	This pin is used to supply DC bias to the VCO, prescaler, and PLL. An IF bypass capacitor should be connected directly to this pin and returned to ground. A 10nF capacitor is recommended for 10.7MHz IF applications.	
28	GND4	GND4 is the ground shared on chip by the VCO, prescaler, and PLL electronics.	

11 TRANSCEIVERS

RF2917

Pin	Function	Description	Interface Schematic
29	LOOP FLT	Output of the charge pump, and input to the VCO control. An RC network from this pin to ground is used to establish the PLL bandwidth.	
30	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 100pF capacitor should be connected between pin 30 and pin 31.	
31	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 100pF capacitor should be connected from this pin to ground.	See pin 30.
32	PD	This pin is used to power up or down the RF2917. A logic high (PWR DWN >2.0V) powers up the receiver and PLL. A logic low (PWR DWN <1.0V) powers down circuit to standby mode.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 3, 5, 7-19, 21-24, 27-31.