C. DOCUMENTATION TECHNIQUE

Annexe A1

Extraits de la documentation constructeur de l'accéléromètre LIS331DLH.

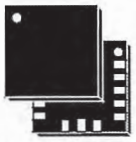
Description générale

LIS331DLH

MEMS digital output motion sensor
ultra low-power high performance 3-axes "nano" accelerometer

Features

- Wide supply voltage, 2.16 V to 3.6 V
- Low voltage compatible IOs, 1.8 V
- Ultra low-power mode consumption down to 10 µA
- ±2*g*/±4*g*/±8*g* dynamically selectable full-scale
- I^2C/SPI digital output interface
- 16 bit data output
- 2 independent programmable interrupt generators for free-fall and motion detection
- Sleep to wake-up function
- 6D orientation detection
- Embedded self-test
- 10000 *g* high shock survivability
- ECOPACK® RoHS and "Green" compliant (see *Section 8*)



LGA 16 (3x3x1 mm)

Applications

- Motion activated functions
- Free-fall detection
- Intelligent power saving for handheld devices
- Pedometer
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LIS331DLH is an ultra low-power high performance three axes linear accelerometer belonging to the "nano" family, with digital I^2C/SPI serial interface standard output.

The device features ultra low-power operational modes that allow advanced power saving and smart sleep to wake-up functions.

The LIS331DLH has dynamically user selectable full scales of ±2*g*/±4*g*/±8*g* and it is capable of measuring accelerations with output data rates from 0.5 Hz to 1 kHz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The device may be configured to generate interrupt signal by inertial wake-up/free-fall events as well as by the position of the device itself. Thresholds and timing of interrupt generators are programmable by the end user on the fly.

The LIS331DLH is available in small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temperature range [° C]	Package	Packaging
LIS331DLH	-40 to +85	LGA 16	Tray
LIS331DLHTR	-40 to +85	LGA 16	Tape and reel

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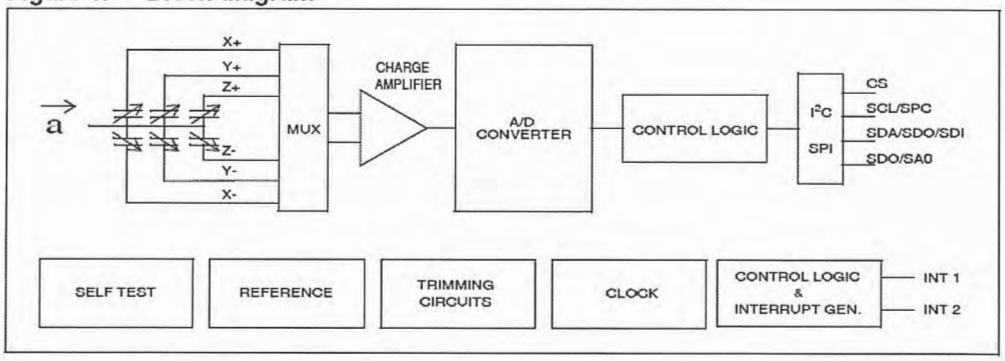
1 Block diagram and pin description

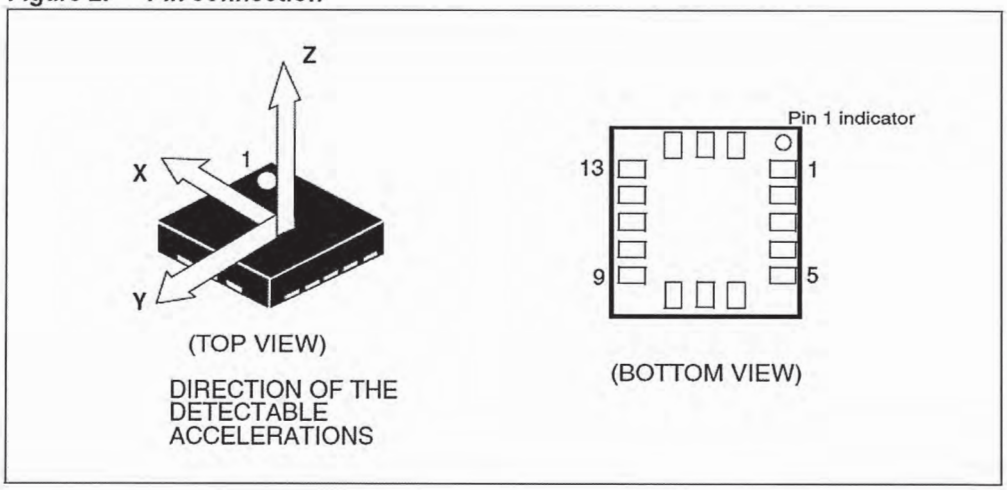
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection



Plage de mesure et de sensibilité, en fonction de la valeur stockée dans les bits FS1 et FS0 du registre CTRL_REG4(23h) :

Table 3. Mechanical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted (1)

Symbol	Parameter	Test conditions	Min.	Typ.(2)	Max.	Unit
FS	Measurement range(3)	FS bit set to 00		±2.0		*g*
		FS bit set to 01		±4.0		
		FS bit set to 11		±8.0		
So	Sensitivity	FS bit set to 00 12 bit representation	0.9	1	1.1	m*g*/digit
		FS bit set to 01 12 bit representation	1.8	2	2.2	
		FS bit set to 11 12 bit representation	3.5	3.9	4.3	
TCSo	Sensitivity change vs temperature	FS bit set to 00		±0.01		%/°C
TyOff	Typical zero-*g* level offset accuracy(4),(5)	FS bit set to 00		±20		m*g*
TCOff	Zero-*g* level change vs temperature	Max delta from 25 °C		±0.1		m*g*/°C
An	Acceleration noise density	FS bit set to 00		218		$\mu g/\sqrt{Hz}$
Vst	Self-test output change(6),(7),(8)	FS bit set to 00 X axis	120	300	550	LSb
		FS bit set to 00 Y axis	120	300	550	LSb
		FS bit set to 00 Z axis	140	350	750	LSb
Top	Operating temperature range		-40		+85	°C
Wh	Product weight			20		mgram

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.
2. Typical specifications are not guaranteed
3. Verified by wafer level test and measurement of initial offset and sensitivity
4. Typical zero-*g* level offset value after MSL3 preconditioning
5. Offset can be eliminated by enabling the built-in high pass filter
6. The sign of "Self-test output change" is defined by CTRL_REG4 STsign bit (*Table 28*), for all axes.
7. Self-test output changes with the power supply. "Self-test output change" is defined as $OUTPUT[LSb]_{(CTRL\_REG4\ ST\ bit=1)}$ - $OUTPUT[LSb]_{(CTRL\_REG4\ ST\ bit=0)}$. 1LSb=4*g*/4096 at 12bit representation, ±2 *g* Full-scale
8. Output data reach 99% of final value after 1/ODR+ 1 ms when enabling self-test mode, due to device filtering

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Registre de stockage des accélérations mesurées sur les axes X, Y et Z (en complément à 2, représentation sur 16 bits) :

Table 15. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00 - 0E			Reserved
WHO_AM_I	r	0F	000 1111	00110010	Dummy register
Reserved (do not modify)		10 - 1F			Reserved
CTRL_REG1	rw	20	010 0000	00000111	
CTRL_REG2	rw	21	010 0001	00000000	
CTRL_REG3	rw	22	010 0010	00000000	
CTRL_REG4	rw	23	010 0011	00000000	
CTRL_REG5	rw	24	010 0100	00000000	
HP_FILTER_RESET	r	25	010 0101		Dummy register
REFERENCE	rw	26	010 0110	00000000	
STATUS_REG	r	27	010 0111	00000000	
OUT_X_L	r	28	010 1000	output	
OUT_X_H	r	29	010 1001	output	
OUT_Y_L	r	2A	010 1010	output	
OUT_Y_H	r	2B	010 1011	output	
OUT_Z_L	r	2C	010 1100	output	
OUT_Z_H	r	2D	010 1101	output	
Reserved (do not modify)		2E - 2F			Reserved
INT1_CFG	rw	30	011 0000	00000000	
INT1_SOURCE	r	31	011 0001	00000000	
INT1_THS	rw	32	011 0010	00000000	
INT1_DURATION	rw	33	011 0011	00000000	
INT2_CFG	rw	34	011 0100	00000000	
INT2_SOURCE	r	35	011 0101	00000000	
INT2_THS	rw	36	011 0110	00000000	
INT2_DURATION	rw	37	011 0111	00000000	
Reserved (do not modify)		38 - 3F			Reserved

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

Rôle fonctionnel des entrées et des sorties :

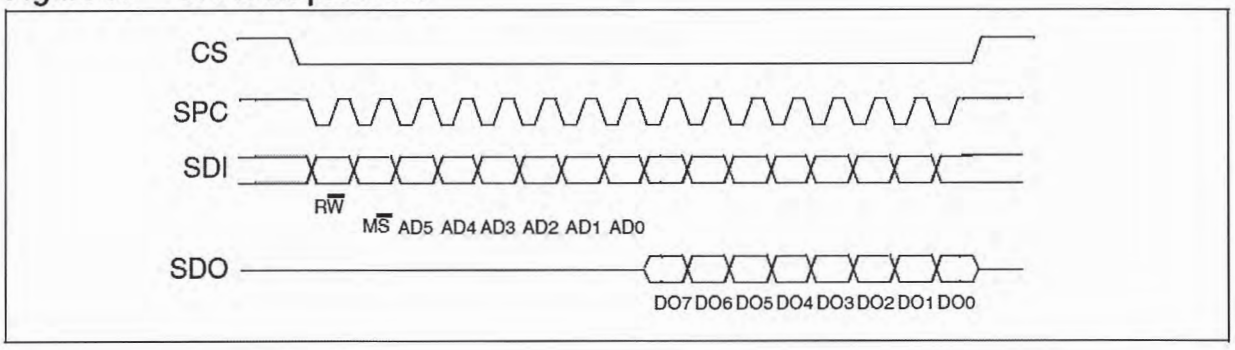
Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not connected
3	NC	Not connected
4	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0V supply
6	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
8	CS	SPI enable I²C/SPI mode selection (1: I²C mode; 0: SPI enabled)
9	INT 2	Inertial interrupt 2
10	Reserved	Connect to GND
11	INT 1	Inertial interrupt 1
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	Reserved	Connect to Vdd
16	GND	0 V supply

Procédure de lecture de l'accélération Ax sur la liaison SPI :

La communication entre l'accéléromètre et le microcontrôleur, sur le bus SPI, lors de la lecture de plusieurs octets est décrite sur le chronogramme ci-dessous.

Figure 7. SPI read protocol



Cas particulier « multibyte read sequence » :

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The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

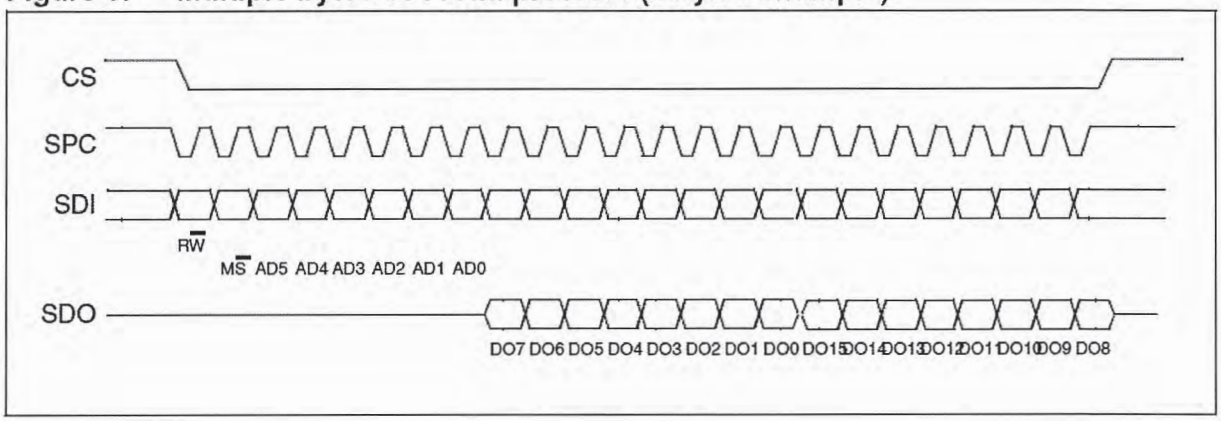
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 8. Multiple bytes SPI read protocol (2 bytes example)



Annexe A2

Extraits de la documentation technique de l'amplificateur opérationnel LF357.

DC Electrical Characteristics

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25°C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (2)		0.5			0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_J=25°C, (1) (3)		3	20		3	20		3	50	pA
		$T_J \le T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	T_J=25°C, (1) (3)		30	100		30	100		30	200	pA
		$T_J \le T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1		±11	±15.1		+10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(4)	85	100		85	100		80	100		dB

(1) Unless otherwise stated, these test conditions apply:

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	±15V ≤ V_S ≤ ±20V	±15V ≤ V_S ≤ ±20V	±15V ≤ V_S ±20V	V_S= ±15V
T_A	−55°C ≤ T_A ≤ +125°C	−25°C ≤ T_A ≤ +85°C	0°C ≤ T_A ≤ +70°C	0°C ≤ T_A ≤ +70°C
T_{HIGH}	+125°C	+85°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

(2) The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

(4) Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

DC Electrical Characteristics

$T_A = T_J$ = 25°C, V_S = ±15V

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

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AC Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/ 356B	LF156/256/356/ LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/µs
		LF357: A_V=5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(1)	4		1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	nV/√Hz
		f=1000 Hz	20		12	12	nV/√Hz
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	pA/√Hz
		f=1000 Hz	0.01		0.01	0.01	pA/√Hz
C_{IN}	Input Capacitance		3		3	3	pF

(1) Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, A_V = −5, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

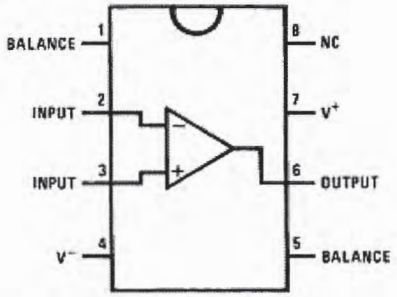


Figure 35. SOIC and PDIP Package (D and P)
See Package Number
D (R-PDSO-G8) or P (R-PDIP-T8)

Annexe A3

Extraits de la documentation technique du convertisseur AD7530 :

intersil

AD7520, AD7530, AD7521, AD7531

August 1997

10-Bit, 12-Bit, Multiplying D/A Converters

Features

- **AD7520/AD7530, 10-Bit Resolution; 8-Bit, 9-Bit and 10-Bit Linearity**
- **AD7521/AD7531, 12-Bit Resolution; 8-Bit, 9-Bit and 10-Bit Linearity**
- **Low Power Dissipation (Max) 20mW**
- **Low Nonlinearity Tempco at 2ppm of FSR/°C**
- **Current Settling Time to 0.05% of FSR 1.0µs**
- **Supply Voltage Range . . . . . ±5V to +15V**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

Description

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Intersil' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

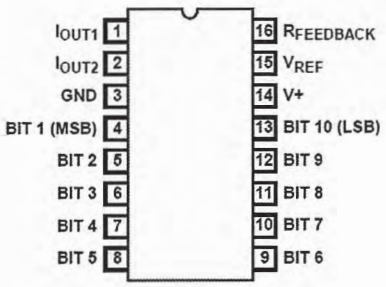
The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

Ordering Information

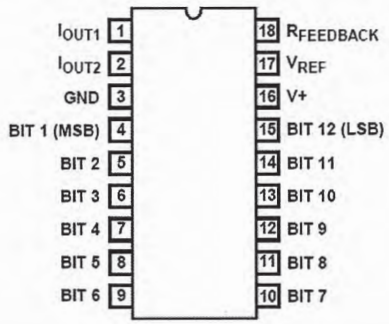
PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
AD7520JN, AD7530JN	0.2% (8-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7520KN, AD7530KN	0.1% (9-Bit)	0 to 70	16 Ld PDIP	E16.3
AD7521JN, AD7531JN	0.2% (8-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7521KN, AD7531KN	0.1% (9-Bit)	0 to 70	18 Ld PDIP	E18.3
AD7520LN, AD7530LN	0.05% (10-Bit)	-40 to 85	16 Ld PDIP	E16.3
AD7521LN, AD7531LN	0.05% (10-Bit)	-40 to 85	18 Ld PDIP	E18.3
AD7520JD	0.2% (8-Bit)	-25 to 85	16 Ld CERDIP	F16.3
AD7520KD	0.1% (9-Bit)	-25 to 85	16 Ld CERDIP	F16.3
AD7520LD	0.05% (10-Bit)	-25 to 85	16 Ld CERDIP	F16.3
AD7520SD, AD7520SD/883B	0.2% (8-Bit)	-55 to 125	16 Ld CERDIP	F16.3
AD7520UD, AD7520UD/883B	0.05% (10-Bit)	-55 to 125	16 Ld CERDIP	F16.3

Pinouts

AD7520, AD7530
(CERDIP, PDIP)
TOP VIEW



AD7521, AD7531
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3104.1**

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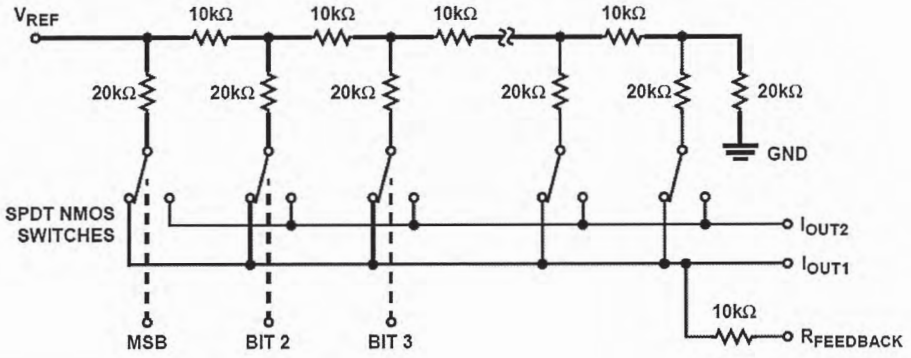
Functional Diagram



NOTES:

Switches shown for Digital Inputs "High".

Resistor values are typical.

Electrical Specifications V+ = +15V, V_{REF} = +10V, T_A = 25°C Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE (Note 2)									
Resolution			10	10	10	12	12	12	Bits
Nonlinearity	J, S	S Over -55°C to 125°C (Notes 2, 5) (Figure 3)	-	-	±0.2 (8-Bit)	-	-	±0.2 (8-Bit)	% of FSR
	K	T Over -55°C to 125°C (Figure 2)	-	-	±0.1 (9-Bit)	-	-	±0.1 (9-Bit)	% of FSR
	L, U	-10V ≤ V_{REF} ≤ +10V U Over -55°C to 125°C (Figure 2)	-	-	±0.05 (10-Bit)	-	-	±0.05 (10-Bit)	% of FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V (Notes 3, 4)	-	-	±2	-	-	±2	ppm of FSR/°C
Gain Error			-	±0.3	-	-	±0.3	-	% of FSR
Gain Error Tempco			-	-	±10	-	-	±10	ppm of FSR/°C
Output Leakage Current (Either Output)		Over the Specified Temperature Range	-	-	±200 (±300)	-	-	±200 (±300)	nA
DYNAMIC CHARACTERISTICS									
Output Current Settling Time		To 0.05% of FSR (All Digital Inputs Low To High And High To Low) (Note 4) (Figure 7)	-	1.0	-	-	1.0	-	µs
Feedthrough Error		V_{REF} = 20V_{P-P}, 10kHz (50kHz) All Digital Inputs Low (Note 4) (Figure 6)	-	-	10	-	-	10	mV_{P-P}
REFERENCE INPUT									
Input Resistance		All Digital Inputs High I_{OUT1} at Ground	5	10	20	5	10	20	kΩ
ANALOG OUTPUT									
Output Capacitance	I_{OUT1}	All Digital Inputs High (Note 4) (Figure 5)	-	200	-	-	200	-	pF
	I_{OUT2}		-	75	-	-	75	-	pF
	I_{OUT1}	All Digital Inputs Low (Note 4) (Figure 5)	-	75	-	-	75	-	pF
	I_{OUT2}		-	200	-	-	200	-	pF

Electrical Specifications V+ = +15V, V_{REF} = +10V, T_A = 25°C Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Noise	Both Outputs (Note 4) (Figure 4)	-	Equivalent to 10kΩ	-	-	Equivalent to 10kΩ	-	Johnson Noise
DIGITAL INPUTS								
Low State Threshold, V_{IL}	Over the Specified Temperature Range V_{IN} = 0V or +15V	-	-	0.8	-	-	0.8	V
High State Threshold, V_{IH}		2.4	-	-	2.4	-	-	V
Input Current, I_{IL}, I_{IH}		-	-	±1	-	-	±1	µA
Input Coding	See Tables 1 and 2	Binary/Offset Binary						
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection	V+ = 14.5V to 15.5V (Note 3) (Figure 3)	-	±0.005	-	-	±0.005	-	% FSR/ % ΔV+
Power Supply Voltage Range		+5 to +15			+5 to +15			V
I+	All Digital Inputs at 0V or V+ Excluding Ladder Network	-	±1	-	-	±1	-	µA
	All Digital Inputs High or Low Excluding Ladder Network	-	-	2	-	-	2	mA
Total Power Dissipation	Including the Ladder Network	-	20	-	-	20	-	mW

NOTES:

2. Full scale range (FSR) is 10V for Unipolar and ±10V for Bipolar modes.
3. Using internal feedback resistor $R_{FEEDBACK}$.
4. Guaranteed by design, or characterization and not production tested.
5. Accuracy not guaranteed unless outputs at GND potential.
6. Accuracy is tested and guaranteed at V+ = 15V only.

Modèle ENSD ©NEOPTEC

Nom :
(Suivi, s'il y a lieu, du nom d'épouse)

Prénom :

N° d'inscription :

(Le numéro est celui qui figure sur la convocation ou la feuille d'émargement)

Né(e) le : / /

Concours	Section/Option	Epreuve	Matière

DR1 - DR2 - DR3

Document réponse DR1

Associé à la partie I, Q3

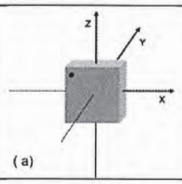
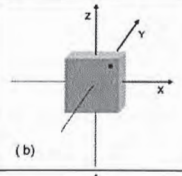
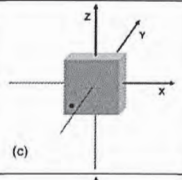
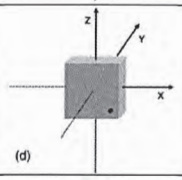
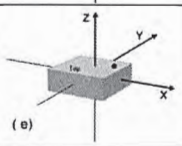
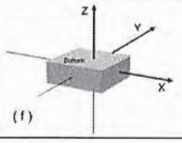
Code C++ ci-dessous à compléter (au niveau encadré):

```
Bool C_CCD ::extract_CCD_img(void)
{
int x,y ;

for (x=0 ;x<640 ; x++)
        {
        for (y=0 ; y<480 ; y++)
                {



                img_in[…][…]=



                } ;

        } ;
return TRUE ;
}
```

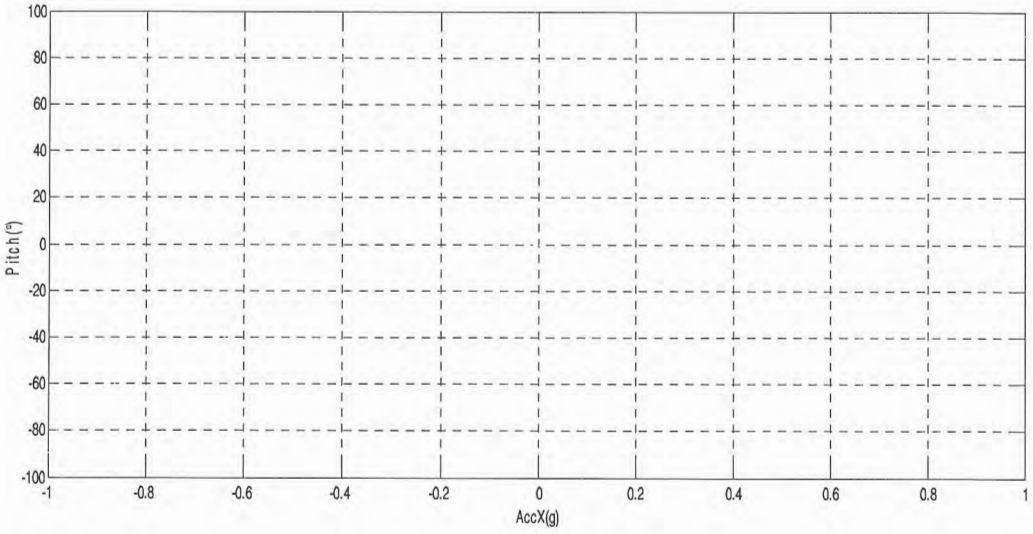
Document réponse DR2

Associé à la partie II, Q13 et Q14.

Q13 :

Ligne	Position	Accélération sur X_C	Accélération sur Y_C	Accélération sur Z_C
1	 (a)	-1g ☐ 0g x☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐x	-1g ☐ 0g ☐x +1g ☐
2	 (b)	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐
3	 (c)	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐
4	 (d)	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐
5	 (e)	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐
6	 (f)	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐	-1g ☐ 0g ☐ +1g ☐

Q14 :



Tournez la page S.V.P.

Document réponse DR3

Associé à la partie II, Q18

Valeurs d'accélération sur axe X_C	Valeur de FS1..0	OUT_X_H (hexa)	OUT_X_L (hexa)
0g	00		
350mg	00		
1g	00		
-350mg	00		
-1g	11		

Tableau 2. Valeurs stockées dans l'accéléromètre

Modèle ENSD ©NEOPTEC

Nom :
(Suivi, s'il y a lieu, du nom d'épouse)

Prénom :

N° d'inscription :

(Le numéro est celui qui figure sur la convocation ou la feuille d'émargement)

Né(e) le : / /

Concours	**Section/Option**	**Epreuve**	**Matière**

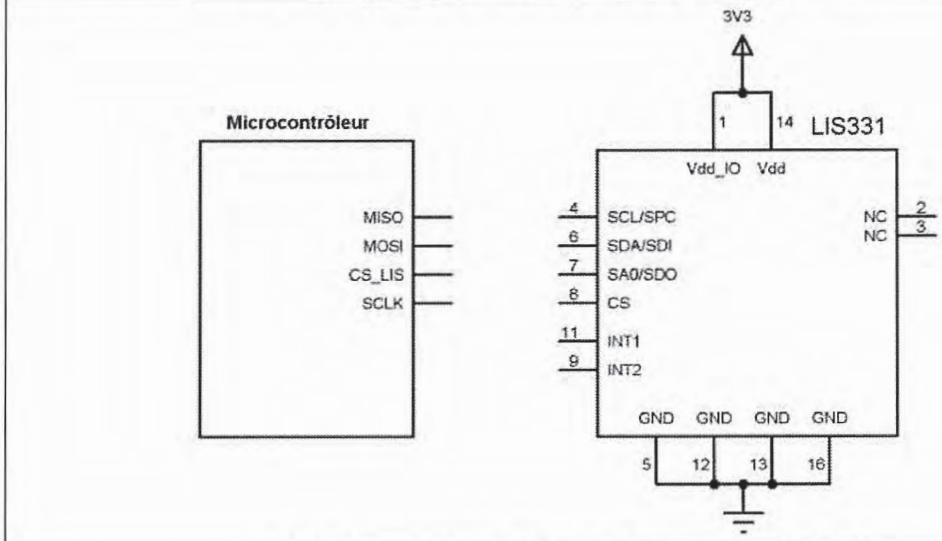
DR4 - DR5

Document réponse DR4

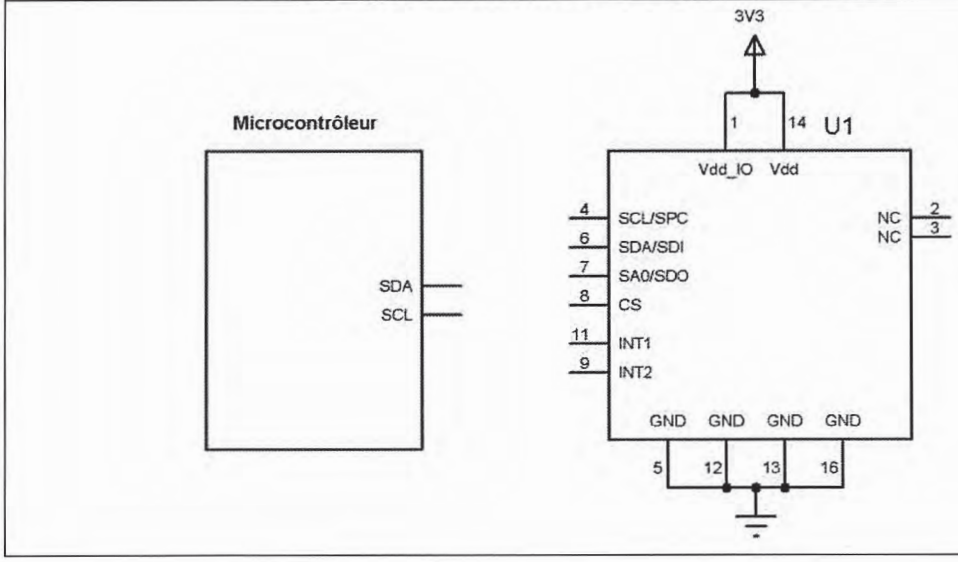
Associé à la partie II, Q19, Q20 et Q22.

Q19 & Q20 :

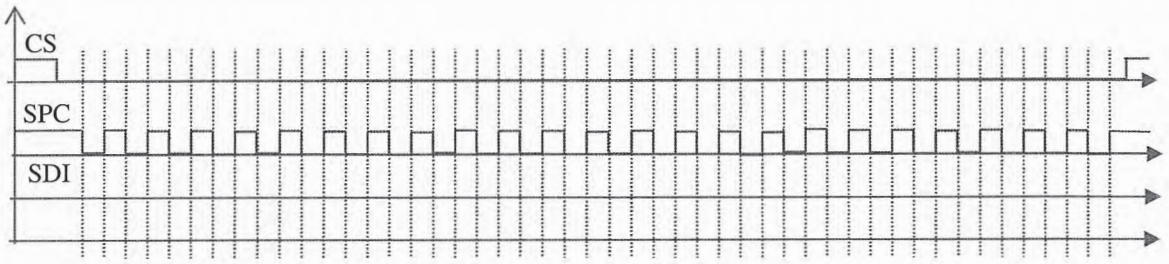
Câblage de l'accéléromètre en mode SPI



Câblage de l'accéléromètre en mode I2C



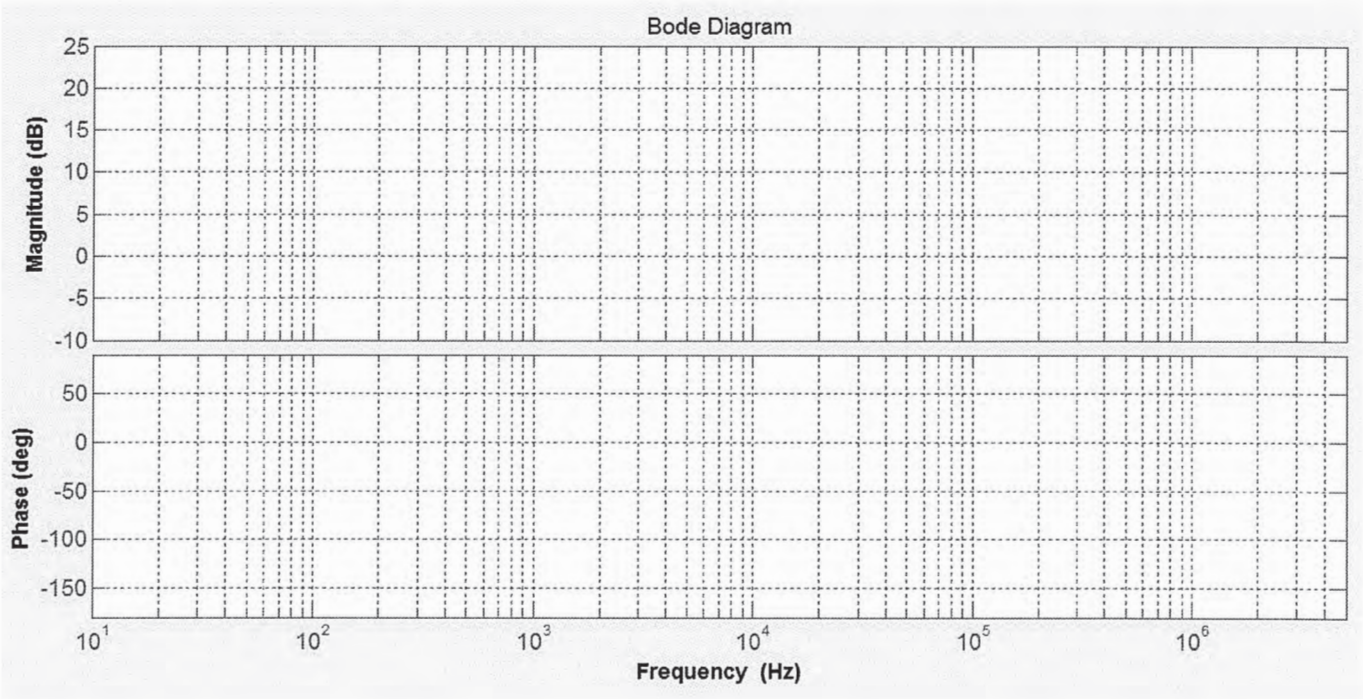
Q22:



Document réponse DR5

Associé à la partie III, Q41 & Q43.

Q41 : Diagramme de Bode asymptotique en module et en phase de la transmittance en boucle fermée T(p).



Q43 : Diagramme de Bode asymptotique en module et en phase de la transmittance C(p).