RF2917 Theory of Operation and Application Information

The RF2917 is part of a family of low-power RF transceiver IC's developed for wireless data communication devices operating in the European 433/868MHz ISM bands or the U.S. 915MHz ISM band. This IC has been implemented in a 15GHz silicon bipolar process technology that allows low-power transceiver operation in a variety of commercial wireless products. The RF2917 realizes a highly integrated, single-conversion FM/FSK receiver with the addition of a reference crystal, intermediate frequency (IF) filtering, and a few passive components. The LNA (low noise amplifier) input of the RF2917 is easily matched to a front-end filter or antenna by means of a DC blocking capacitor and reactive components. The receiver local oscillator (LO) is generated by an internalized VCO, PLL and phase discriminator in conjunction with the external reference crystal, loop filter and VCO resonator components. The receiver IF section is optimized to interface with low cost 10.7MHz ceramic filters, and its -3dB bandwidth of 25MHz also allows it to be used (with lower gain) at higher frequencies with other types of filters.

FM/FSK SYSTEMS

The receiver output functionality is determined by the tri-state MUTE input. The three output configurations are linear FM, FSK and mute. An on-chip 1.6MHz RC filter, which follows the demodulator output, filters the harmonics of the IF signal from the output data.

When in the FM mode, the FM OUT signal is the buffered output from the quadrature demodulator. The output signal has a fixed DC offset of V_{CC}-1.0V, while the AC level is dependent on the FM deviation, with a maximum level of 240mV$_{P-P}$ For optimum operation in either FM or FSK mode, FM deviation needs to exceed (with margin) the carrier frequency error anticipated between the receiver and transmitter.

When in the FSK mode, the FM OUT signal is clipped, having a rail-to-rail output level. The FM OUT pin is only capable of driving rail-to-rail output into a very high impedance and small capacitance, with the amount of capacitance determining the FM OUT bandwidth. For a 3pF load, the bandwidth is in excess of 500kHz. The rail-to-rail output is also limited by the frequency deviation and bandwidth of the IF filters. With the 180kHz bandwidth filters on the evaluation boards, the rail-to-rail output is limited to less than 140kHz. Choosing the right IF bandwidth and deviation versus data rate (modulation index) is important in evaluating the applicability of the RF2917 for a given data rate.

AM SYSTEMS

The RF2919 is recommended for use in ASK/OOK applications, however, the RF2917 may be utilized in an AM system by using the RSSI (received signal strength indicator) output to recover the modulation. The FM output mode should be selected for AM operation because of the higher RSSI resolution in FM mode.

RSSI

The RSSI output signal is supplied from a current source and therefore requires a resistor to convert it to a voltage. The RSSI is linear over the same range of input power for both FM and FSK modes, but the FM mode has higher RSSI resolution. For a 51kΩ resistive load, the RSSI will range from 1.0V to 2.6V in FM mode and from 0.8V to 1.5V in FSK mode (3.6V supply). A small parallel capacitor is suggested to limit the bandwidth and filter noise.

APPLICATION AND LAYOUT CONSIDERATIONS

The RX IN pin is DC-biased, requiring a DC blocking capacitor. If the RF filter has DC blocking characteristics, such as a ceramic dielectric filter, then a DC blocking capacitor is not necessary. When in power down mode, the RX IN impedance increases. Therefore, in a half-duplex application, the RF2917 RX IN may share the RF filter with a transmitter output having a similar high impedance power down characteristic. Care must be taken in this case to account for loading effects of the transmitter on the receiver, and vice versa, in matching the filter to both the transmitter and receiver.

The VCO is a very sensitive block in this system. RF signals feeding back into the VCO by either radiation or coupling of traces may cause the PLL to become unlocked. The trace(s) for the anode of the tuning varactor should also be kept short. The layout of the resonators and varactor are very important. The capacitor and varactor should be closest to the RF2917 pins and the trace length should be as short as possible. The inductors can be placed further away and any trace inductance can be compensated by reducing the value of the inductors. Printed inductors may also be used with careful design. For best results, the physical layout should be as symmetrical as possible.

When using loop bandwidths lower than the 5kHz shown on the evaluation board, better supply filtering at the resonators (and lower V_{CC} noise as well) will help reduce the phase noise of the VCO; a series resistor of 100Ω to 200Ω and a 1μF or larger capacitor

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may be used. Phase noise is generally more critical in narrowband applications where adjacent channel selectivity is a concern, but it can also contribute to raising the noise floor of the receiver, thereby degrading sensitivity.

For the interface between the LNA and mixer, the coupling capacitor should be as close to the RF2917 pins as possible, with the bias inductor being further away. Once again, the value of the inductor may be changed to compensate for trace inductance. The output impedance of the LNA is on the order of several kΩ, which makes matching to 50Ω difficult. If image filtering is desired, a high impedance filter is recommended. If no filtering is used, the match to the mixer input need not be a good conjugate match, because of the high gain of the IF amplifier stages. In fact, a conjugate match between the LNA and mixer will not significantly improve sensitivity, but will have an adverse effect on system IIP3 and increase the likelihood of IF instability.

Because of the high gain of the IF section, care should be taken in laying out the IF filtering and discriminator components to minimize the possibility of instability. In particular, inductive feedback may occur between the inductor of a discrete (LC) discriminator and any inductor(s) in the IF interstages. Orthogonal placement of inductors will generally minimize coupling. Indicators that an instability may exist include poor sensitivity and a high RSSI level when no input signal is present.

The quadrature tank of the discriminator may be implemented with ceramic discriminators available from a variety of sources. This design works well for wideband applications, and where the temperature range is limited. The temperature coefficient of a ceramic discriminator may be on the order of ±50ppm/°C. An automatic frequency control loop may be implemented using the DC level of the FM OUT for feedback to an external varactor on the reference crystal. An alternative to the ceramic discriminator is an LC tank. The DEMOD IN pin has a DC bias and must be DC-blocked. This can be done either at the pin or at the ground side of the LC tank (this must also be done if a parallel resistor is used with a ceramic discriminator). The decision whether to use an LC or a ceramic discriminator should be based on the frequency deviation in the system, discriminator Q needed, and frequency and temperature tolerances. Tuning of the LC tank is required to overcome the component tolerances in the tank.

PREDICTING AND MINIMIZING PLL LOCK TIME

The RF2917 implements a conventional on-chip PLL. The VCO is followed by a prescaler, which divides down the output frequency for comparison with the reference oscillator frequency. The output of the phase discriminator is a sequence of pulse width modulated current pulses in the required direction to steer the VCO's control voltage to maintain phase lock, with a loop filter integrating the current pulses. The lock time of this PLL is a combination of the loop transient response time and the slew rate set by the phase discriminator output current, combined with the magnitude of the loop filter capacitance. A good approximation for total lock time of the RF2917 is:

$$LockTime = \frac{D}{F_C} + 35000 \cdot C \cdot dV$$

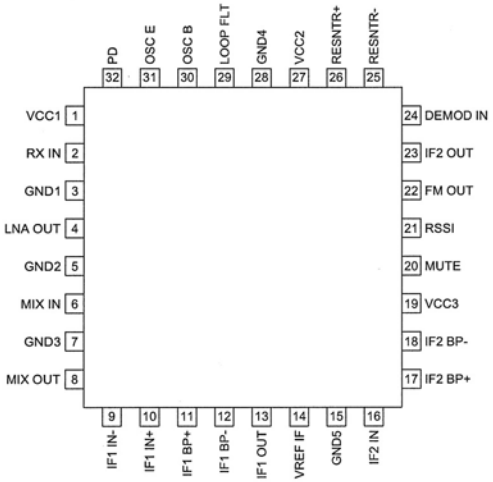
where D is a factor to account for the loop damping, F_C is the loop cut frequency, C is the sum of all shunt capacitors in the loop filter, and dV is the required step voltage change to produce the desired frequency change during the transient. For loops with low phase margin (30° to 40°), use D=2, whereas for loops with better phase margin (50° to 60°), use D=1.

To lock faster, C needs to be minimized.

1. Design the loop filter for the minimum phase margin possible without causing loop instability problems; this allows C to be kept at a minimum.

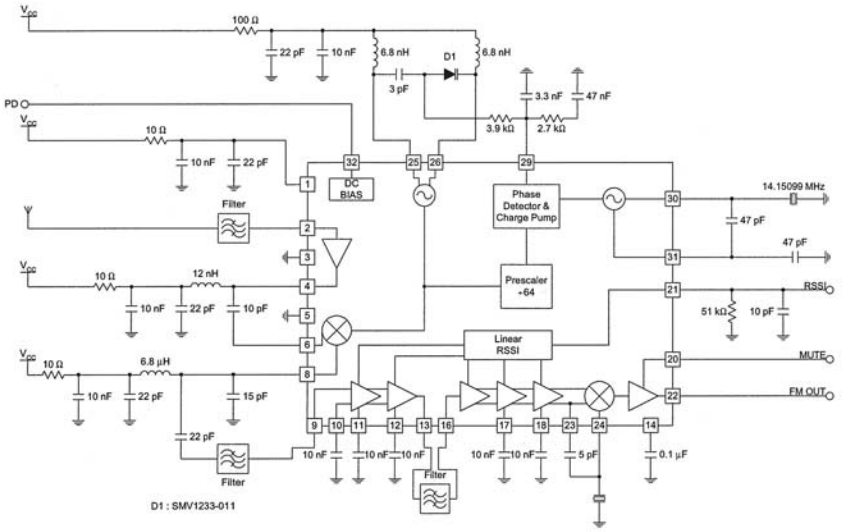
2. Design the loop filter for the highest loop cut frequency possible without distorting low frequency modulation components; this also allows C to be kept at a minimum.

Pin Out



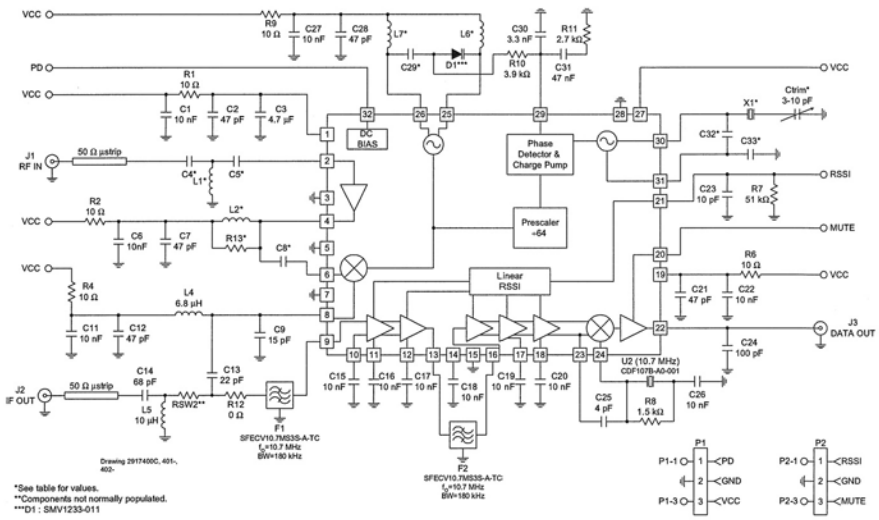
RF2917

915MHz Application Schematic



Evaluation Board Schematic
H (915MHz), M (868MHz), L (433MHz) boards

(Download Bill of Materials from www.rfmd.com.)



Board	C4 (pF)	L1 (nH)	C5 (pF)	L2 (nH)	R13 (Ω)	C8 (pF)	L6 (nH)	L7 (nH)	C29 (pF)	X1 (MHz)	C32 (pF)	C33 (pF)
L (433MHz)	2	27	100	33	510	9	18	18	9	6.612813	100	100
M (868MHz)	1.5	8.2	100	12	-	1	6.8	6.8	3	13.41015	100	100
H (915MHz)	2	6.8	22	12	-	1	6.8	6.8	3	14.15099	47	47

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CRYSTAL
Semiconductor Corporation

CS4215

16-Bit Multimedia Audio Codec

Features

- Sample Frequencies from 4 kHz to 50 kHz
- 16-bit Linear, 8-bit Linear, μ-Law, or A-Law Audio Data Coding
- Programmable Gain for Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Level Analog Inputs
- Headphone, Speaker, and Line Outputs
- On-chip Anti-Aliasing/Smoothing Filters
- Serial Digital Interface

General Description

mwave The CS4215 is an Mwave™ audio codec.

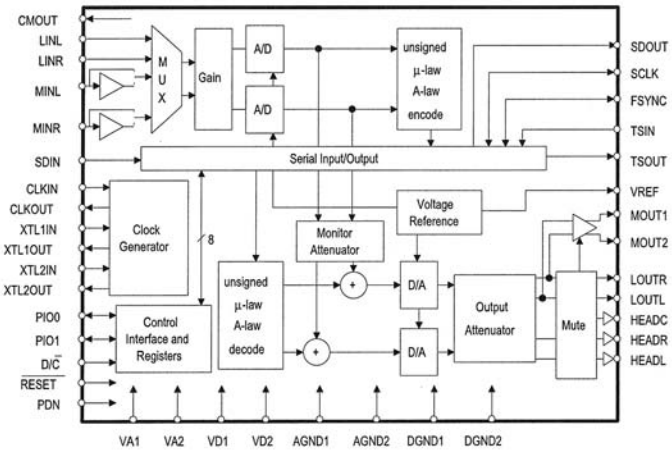
The CS4215 is a single-chip, stereo, CMOS multimedia codec that supports CD-quality music, FM radio-quality music, telephone-quality speech, and modems. The analog-to-digital and digital-to-analog converters are 64×oversampled delta-sigma converters with on-chip filters which adapt to the sample frequency selected.

The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker driver, results in a very small footprint.

Ordering Information:

CS4215-KL	0°C to 70°C	44-pin PLCC
CS4215-KQ	0°C to 70°C	100-pin TQFP
CDB4215	Evaluation Board	



This data sheet was written for Revision E CS4215 codecs and later. For differences between Revision E and previous versions, see *Appendix A.*

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = +5V;

Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2; Full Scale Input Sine wave, No Gain, No Attenuation 1 kHz; Conversion Rate = 48 kHz; No Gain, No Attenuation, SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Slave mode; Unless otherwise specified.)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution			16	-	-	Bits
ADC Differential Nonlinearity			-	-	±0.9	LSB
Instantaneous Dynamic Range	Line Inputs Mic Inputs	IDR	80 72	84 78	- -	dB dB
Total Harmonic Distortion	Line Inputs Mic Inputs	THD	- -	- -	0.012 0.032	% %
Interchannel Isolation	Line to Line Inputs Line to Mic Inputs		- -	80 60	- -	dB dB
Interchannel Gain Mismatch	Line Inputs Mic Inputs		- -	- -	0.5 0.5	dB dB
Frequency Response (Note 1)	(0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Input Gain	Line Inputs Mic Inputs		-0.2 19.8	- -	23.5 44	dB dB
Gain Step Size			-	1.5	-	dB
Absolute Gain Step Error			-	-	0.75	dB
Offset Error with HPF = 0 (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	±150 ±10 ±400	±400 ±150 -	LSB
Offset Error with HPF = 1 (Notes 1,2) (No Gain)	Line Inputs (AC Coupled) Line Inputs (DC Coupled) Mic Inputs		- - -	0 0 0	±5 ±5 ±5	LSB
Full Scale Input Voltage:	(MLB=0) Mic Inputs (MLB=1) Mic Inputs Line Inputs		0.250 2.50 2.50	0.28 2.8 2.8	0.310 3.10 3.10	Vpp V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Input Resistance	(Note 3)		20	-	-	kΩ
Input Capacitance			-	-	15	pF
CMOUT Output Voltage (Maximum output current = 400 µA)	(Note 4)		1.9	2.1	2.3	V

Notes:
1. This specification is guaranteed by characterization, not production testing.
2. Very low frequency signals will be slightly distorted when using the HPF.
3. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance.
4. DC current only. If dynamic loading exists, then CMOUT must be buffered or the performance of ADC's and DAC's may be degraded.

* Parameter definitions are given at the end of this data sheet.

Mwave™ is a trademark of the IBM Corporation.

ANALOG CHARACTERISTICS (Continued)

Parameter *		Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.						
DAC Resolution			16	-	-	Bits
DAC Differential Nonlinearity			-	-	±0.9	LSB
Total Dynamic Range		TDR	-	95	-	dB
Instantaneous Dynamic Range (OLB = 1)	(All Outputs)	IDR	80	85	-	dB
Total Harmonic Distortion (OLB = 1)	Line Out (Note 5) Headphone Out (Note 6) Speaker Out (Note 6)	THD	- - -	- - -	0.025 0.2 0.32	% % %
Interchannel Isolation	Line Out (Note 5) Headphone Out (Note 6)		- -	80 40	- -	dB dB
Interchannel Gain Mismatch	Line Out Headphone		- -	- -	0.5 0.5	dB dB
Frequency Response (Note 1)	(0 to 0.45 Fs)		-0.5	-	+0.2	dB
Programmable Attenuation	(All Outputs)		0.2	-	-94.7	dB
Attenuation Step Size			-	1.5	-	dB
Absolute Attenuation Step Error			-	-	0.75	dB
Offset Voltage	Line Out		-	10	-	mV
Full Scale Output Voltage with OLB = 0	Line Output (Note 5) Headphone Output (Note 6) Speaker Output-Differential (Note 6)		2.55 3.6 7.3	2.8 4.0 8.0	3.08 4.4 8.8	V_{pp} V_{pp} V_{pp}
Full Scale Output Voltage with OLB = 1	Line Output (Note 5) Headphone Output (Note 6) Speaker Output-Differential (Note 6)		1.8 1.8 3.6	2.0 2.0 4.0	2.2 2.2 4.4	V_{pp} V_{pp} V_{pp}
Gain Drift			-	100	-	ppm/°C
Deviation from Linear Phase			-	-	1	Degree
Out of Band Energy	(22 kHz to 100 kHz) Line Out		-	-60	-	dB
Power Supply						
Power Supply Current (Note 7)	Operating Power Down		- -	110 0.5	140 2	mA mA
Power Supply Rejection	(1 kHz)		-	40	-	dB

Notes:
5. 10 kΩ, 100 pF load. Headphone and Speaker outputs disabled.
6. 48 Ω, 100 pF load. For the headphone outputs, THD with 10kΩ, 100pF load is 0.02%.
7. Typically, 50% of the power supply current is supplied to the analog power pins (VA1, VA2) and 50% is supplied to the digital power pins (VD1, VD2). Values given are for unloaded outputs.

A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	s

DIGITAL CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = 5V)

Parameter	Symbol	Min	Max	Units
High-level Input Voltage	V_{IH}	(VD1,VD2)-1.0	(VD1,VD2)+0.3	V
Low-level Input Voltage	V_{IL}	-0.3	1.0	V
High-level Output Voltage at I_O = -2.0 mA	V_{OH}	(VD1,VD2)-0.2	-	V
Low-level Output Voltage at I_O = 2.0 mA	V_{OL}	-	0.1	V
Input Leakage Current (Digital Inputs)		-	10	µA
Output Leakage Current (High-Z Digital Outputs)		-	10	µA

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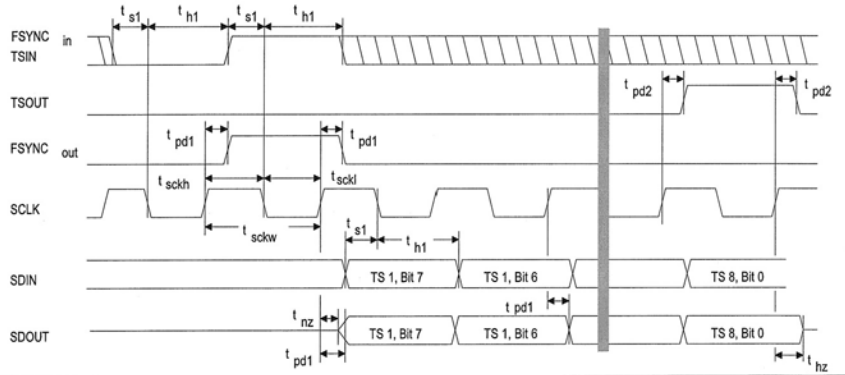
SWITCHING CHARACTERISTICS (T_A = 25°C; VA1, VA2, VD1, VD2 = +5V, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD1, VD2)

Parameter		Symbol	Min	Typ	Max	Units
SCLK period	Master Mode, XCLK = 1 (Note 8)	t_{sckw}	-	1/(Fs*bpf)	-	s
	Slave Mode (XCLK = 0)	tsckw	80	-	-	ns
SCLK high time	Slave Mode, XCLK = 0 (Note 9)	tsckh	25	-	-	ns
SCLK low time	Slave Mode, XCLK = 0 (Note 9)	tsckl	25	-	-	ns
Input Setup Time		t_{s1}	15	-	-	ns
Input Hold Time		t_{h1}	10	-	-	ns
Input Transition Time	10% to 90% points		-	-	10	ns
Output delay		tpd1	-	-	28	ns
SCLK to TSOUT		tpd2	-	-	30	ns
Output to Hi-Z state	Timeslot 8, bit 0	t_{hz}	-	-	12	ns
Output to non-Hi-Z	Timeslot 1, bit 7	t_{nz}	15	-	-	ns
Input Clock Frequency	Crystals		-	-	27	MHz
	CLKIN (Note 10)		1.024	-	13.5	MHz
Input Clock (CLKIN) low time			30	-	-	ns
Input Clock (CLKIN) high time			30	-	-	ns
Sample rate		Fs	4	-	50	kHz
$\overline{\text{RESET}}$ low time	(Note 11)		500	-	-	ns

Notes:
8. In Master mode with BSEL1,0 set to 64 or 128 bits per frame (bpf), the SCLK duty cycle is 50%. When BSEL1,0 is set to 256 bpf, SCLK will have the same duty cycle as CLKOUT. See Internal Clock Generation section.
9. In Slave mode, FSYNC and SCLK must be derived from the master clock running the codec (CLKIN, XTAL1, XTAL2).
10. Sample rate specifications must not be exceeded.
11. After powering up the CS4215, RESET should be held low for 50 ms to allow the voltage reference to settle.



ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

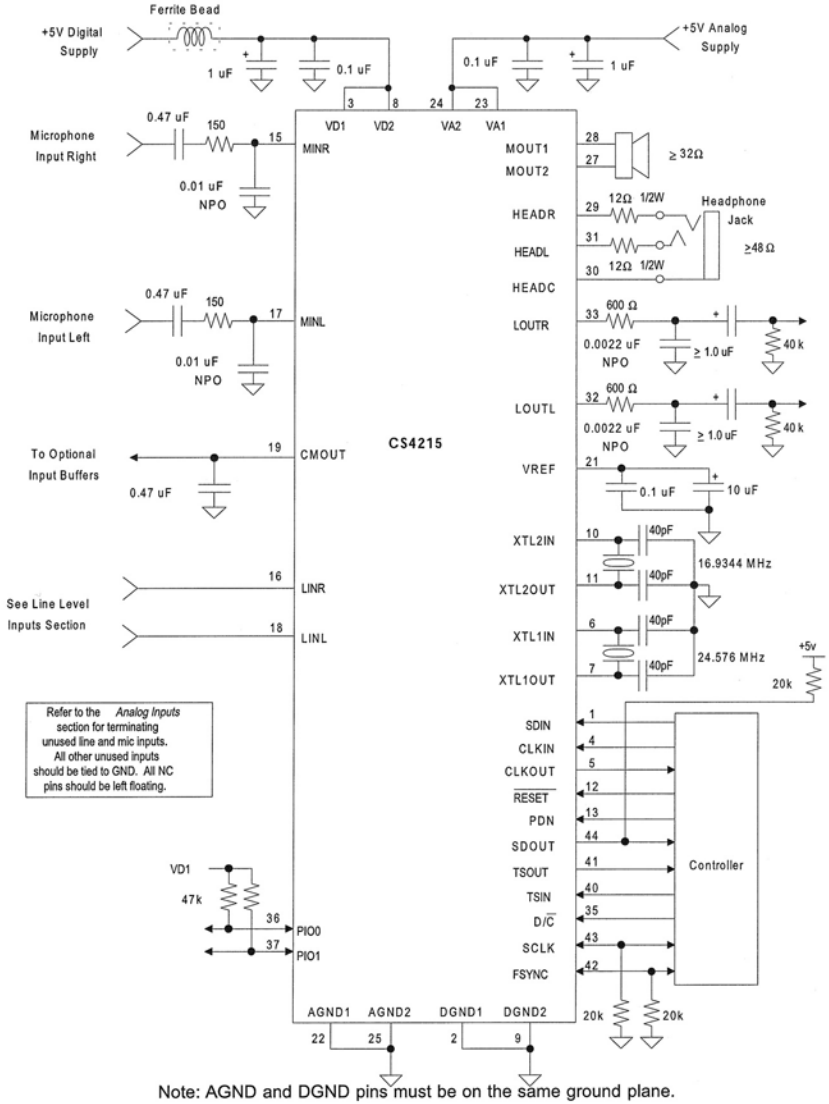
Parameter		Symbol	Min	Max	Units
Power Supplies:	Digital Analog	VD1,VD2 VA1,VA2	-0.3 -0.3	6.0 6.0	V V
Input Current	(Except Supply Pins)		-	±10.0	mA
Analog Input Voltage			-0.3	(VA1, VA2)+0.3	V
Digital Input Voltage			-0.3	(VD1, VD2)+0.3	V
Ambient Temperature	(Power Applied)		-55	+125	°C
Storage Temperature			-65	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter		Symbol	Min	Typ	Max	Units
Power Supplies:	Digital (Note 8) Analog (Note 8)	VD1,VD2 VA1,VA2	4.75 4.75	5.0 5.0	5.25 5.25	V V
Operating Ambient Temperature		T_A	0	25	70	°C

Note: 8. |VD - VA| must be less than 0.5 Volts (one diode drop).



Note: AGND and DGND pins must be on the same ground plane.

Figure 1. Recommended Connection Diagram

FUNCTIONAL DESCRIPTION

Overview

The CS4215 has two channels of 16-bit analog-to-digital conversion and two channels of 16-bit digital-to-analog conversion. Both the ADCs and the DACs are delta-sigma converters. The ADC inputs have adjustable input gain, while the DAC outputs have adjustable output attenuation. Special features include a separate microphone input with a 20 dB programmable gain block, an optional 8-bit µ-law or A-law encoder/decoder, pins for two crystals to set alternative sample rates, direct headphone drive and mono speaker drive.

Control for the functions available on the CS4215, as well as the audio data, are communicated to the device over a serial interface. Separate pins for input and output data are provided, allowing concurrent writing to and reading from the device. Data must be continually written for proper operation. Multiple CS4215 devices may be attached to the same data lines.

Analog Inputs

Figure 1, the recommended connection diagram, shows examples of the external analog circuitry recommended around the CS4215. An internal multiplexer selects between line level inputs and microphone level inputs.

Input filters using a 150 Ω resistor and a .01 µF NPO capacitor to ground are required to isolate the input op-amps from, and provide a charge reserve for, the switched-capacitor input of the codec. The RC values may be safely changed by a factor of two.

The HPF bit in Control Time Slot 2 provides a high pass filter that will reduce DC offset on the analog inputs. Using the high pass filter will cause slight distortions at very low frequencies.

Unused analog inputs that are not selected have a very high input impedance, so they may be tied to AGND directly. Unused analog inputs that are selected should be tied to AGND through a 0.1uF capacitor. This prevents any DC current flow.

Line Level Inputs

LINL and LINR are the line level input pins. These pins are internally biased to the CMOUT voltage. Figure 2 shows a dual op-amp buffer which combines level shifting with a gain of 0.5 to attenuate the standard line level of 2 V_{rms} to

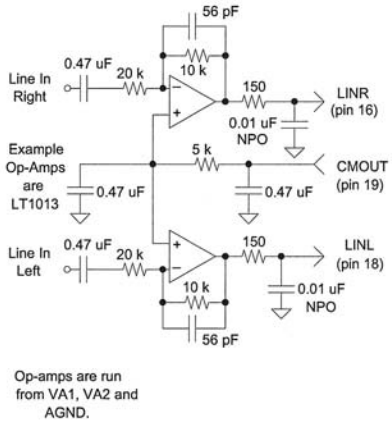


Figure 2. DC Coupled Input.

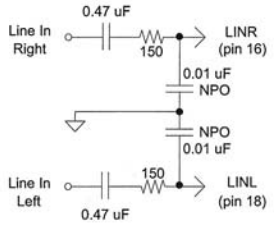


Figure 3. AC Coupled Input.

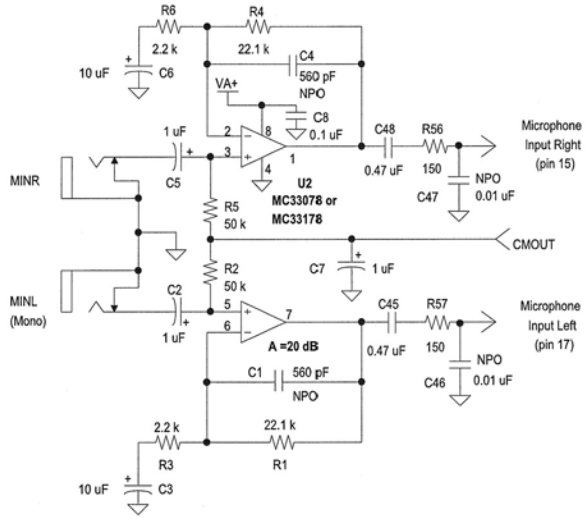


Figure 4. Optional Microphone Input Buffer

1 V_{rms}. The CMOUT reference level is used to level shift the signal. This level shifting allows the line inputs to be DC coupled into the CS4215. Minimum ADC offset results when the line inputs are DC coupled (see Analog Characteristics Table).

Figure 3 shows an AC coupled input circuit for signals centered around 0 Volts. The anti-aliasing RC filter presents a low impedance at high frequencies and should be driven by a low impedance source.

Microphone Level Inputs

Internal amplifiers with a programmable 20 dB gain block are provided for the microphone level inputs, MINR and MINL. Figure 4 shows a single-ended input microphone pre-amplifier stage with a gain of 23 dB. AC coupling is mandatory for these inputs since any DC offset on the input will be amplified by the codec.

The 20 dB gain block may be disabled using the MLB bit in Control Time Slot 1. When disabled, the inputs become line level with full scale inputs of 1 Vrms.

Adjustable Input Gain

The signals from the microphone or the line inputs are routed to a programmable gain circuit which provides up to 22.5 dB of gain in 1.5 dB steps. Level changes only take effect on zero crossings to minimize audible artifacts, often referred to as "zipper noise". The requested level change is forced if no zero crossing is found after 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Analog Outputs

The analog outputs of the DACs are routed via an attenuator to a pair of line outputs, a pair of

headphone outputs and a mono monitor speaker output.

Output Level Attenuator

The DAC outputs are routed through an attenuator, which provides 0 dB to 94.5 dB of attenuation, adjustable in 1.5 dB steps. Level changes are implemented using both analog and digital attenuation techniques. Level changes only take effect on zero crossings to minimize audible artifacts. The requested level change is forced if an analog zero crossing does not occur within 511 frames (10.6 ms at a 48 kHz frame rate). A separate zero crossing detector exists for each channel.

Line Outputs

LOUTR and LOUTL output an analog signal, centered around the CMOUT voltage. The minimum recommended load impedance is 8 kΩ. Figure 1 shows the recommended 1.0 µF DC blocking capacitor with a 40 kΩ resistor to ground. When driving impedances greater than 10 kΩ, this provides a high pass corner of 20 Hz. These outputs may be muted.

Headphone Outputs

HEADR and HEADL output an analog signal, centered around the HEADC voltage. The default headphone output level (OLB = 0) contains an optional 3 dB gain over the line outputs which provides reasonable listening levels, even with small amplitude digital sources. These outputs have increased current drive capability and can drive a load impedance as low as 48 Ω. External 12 Ω series resistors reduce output level variations with different impedance headphones. The common return line from driving headphones should be connected to HEADC, which is biased to the CMOUT voltage. This removes the need for AC coupling, and also controls where the return currents flow. All three headphone output lines are short-circuit protected. These outputs may be muted.

Speaker Output

MOUT1 and MOUT2 differentially drive a small loudspeaker, whose impedance should be greater than 32 Ω. The signal is a summed version of the right and left line output, tapped off prior to the mute function, but after the attenuator. The speaker output may be independently muted. With OLB = 0, the speaker output also contains a 3 dB gain over the line outputs. When OLB = 1, the speaker outputs are driven at the same level as the line outputs.

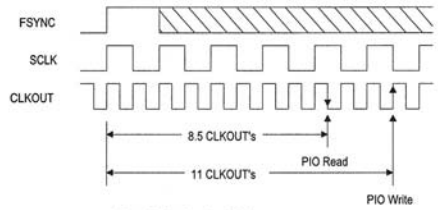
Some small speakers distort heavily when presented with low frequency energy. A high-pass filter helps eliminate the low frequency energy and can be implemented by AC coupling both speaker terminals with a resistor to ground, on the speaker side of the DC blocking capacitors. The values selected would depend on the speaker chosen, but typical values would be 22 µF for the capacitors, with the positive side connected to the codec, and 50 kΩ resistors. This circuit is contained on the CDB4215 evaluation board as shown in the end of this data sheet.

Input Monitor Function

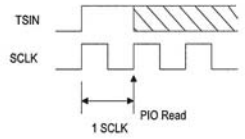
To allow monitoring of the input audio signal, the output of the ADCs can be routed through a monitor path attenuator, then digitally mixed into the input data for the DACs (see the front page block diagram). Changes in the input gain or output level settings directly affect the monitor level. If full scale data from the ADCs is added to full scale digital data from the serial interface, clipping will occur.

Calibration

Both output offset voltage and input offset error are minimized by an internal calibration cycle. At least one calibration cycle must be invoked



Data Mode -Read and Write



Control Mode - Read Only

Notes:
1. DATA MODE READ - The data is sent out via SDOUT on the next frame.
2. CONTROL MODE READ - The data is sent out, via SDOUT, the same frame.
3. DATA MODE READ, WRITE - are tied to the rising edge of FSYNC and CLKOUT. They are independent of SCLK.
4. CONTROL MODE READ - The PIO pins are sampled by a rising edge of SCLK.

Figure 5. PIO Pin Timing

after power up. A calibration cycle will occur immediately after leaving the reset state. A calibration cycle will also occur immediately after going from control mode to data mode (D/$\overline{C}$ going high). When powering up the CS4215, or exiting the power down state, a minimum of 50 ms must occur, to allow the voltage reference to settle, before initiating a calibration cycle. This is achieved by holding $\overline{\text{RESET}}$ low or staying in control mode for 50 ms after power up or exiting power down mode. The input offset error will be calibrated for whichever input channel is selected (microphone or line, using the IS bit). Therefore, the IS bit should remain steady while the codec is calibrating, although the other bits input to the codec are ignored. Calibration takes 194 FSYNC cycles and SDOUT data bits will be zero during this period. The A/D Invalid bit, ADI (bit 7 in data time slot 6), will be high during calibration and will go low when calibration is finished.

Parallel Input/Output

Two pins are provided for parallel input/output. These pins are open drain outputs and require external pull-up resistors. Writing a zero turns on the output transistor, pulling the pin to ground; writing a one turns off the output transistor, which allows an external resistor to pull the pin high. When used as an input, a one must be written to the pin, thereby allowing an external device to pull it low or leave it high. These pins can be read in control mode and their state is recorded in Control Register 5. These pins can be written to and read back in data mode using Data Register 7. Figure 5 shows the Parallel Input/Output timing.

Clock Generation

The master clock operating the CS4215 may be generated using the on-chip crystal oscillators, or by using an external clock source. In all data modes SCLK and FSYNC must be synchronous to the selected master clock.

If the master clock source stops, the digital filters will power down after 5 µs to prevent overheating. If FSYNC stops, the digital filters will power down after approximately 1 FSYNC period. The CS4215 will not enter the total power down state.

Internal Clock Generation

Two external crystals may be attached to the XTL1IN, XTL1OUT, XTL2IN and XTL2OUT pins. Use of an external crystal requires additional 40 pF loading capacitors to digital ground (see Figure 1). XTAL1 oscillator is intended for use at 24.576 MHz and XTAL2 oscillator is intended for use at 16.9344 MHz, although other frequencies may be used. The gain of the internal inverter is slightly higher for XTAL1, ensuring proper operation at >24 MHz frequencies. The crystals should be parallel resonant, fundamental mode and designed for 20 pF loading (equivalent to a 40 pF capacitor on each leg). If XTAL1 or XTAL2 is not selected as the master clock, that particular crystal oscillator is powered down to minimize interference. If a crystal is not needed, the XTL-IN pin should be grounded. An example crystal supplier is CAL Crystal, telephone number (714) 991-1580.

FSYNC and SCLK must be synchronous to the master clock. When using the codec in slave mode with one of the crystals as master clock, the controller must derive FSYNC and SCLK from the crystals, i.e. via CLKOUT. Note that CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low.

An internally generated clock which is 256 times the sample rate (FSYNC rate) is output (CLKOUT) for potential use with an external AES/EBU transmitter, or another CS4215. No glitch occurs on CLKOUT when selecting alternate clock sources. CLKOUT will stop in a low condition within two periods after D/$\overline{C}$ goes low, assuming one of the crystal oscillators is selected, or either CLKIN or SCLK is the master clock source and is continuous. The duty cycle of CLKOUT is 50% if the master clock is one of the crystal oscillators and the DFR bits are 0, 1, 2, 6 or 7. If the DFR bits are 3 or 5, the duty cycle is 33% (high time). If the DFR bits are 4 then CLKOUT has the timing shown in Figure 6. If the master clock is SCLK or CLKIN, the duty cycle of CLKOUT will be the same as the master clock source.

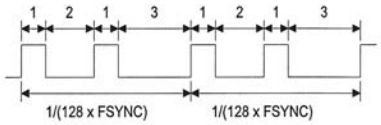


Figure 6. CLKOUT duty cycle using the on-chip crystal oscillator when DFR = 4 (typically FSYNC = 37.8 kHz)

External Clock

An external clock input pin (CLKIN) is provided for potential use with an external AES/EBU receiver, or an already existing system clock. When MCK2 = 0, the input clock must be exactly 256 times the sample rate, and FSYNC and SCLK must be synchronous to CLKIN. When MCK2 = 1 the DFR bits allow various divide ratios off the CLKIN frequency.

Alternatively, an external high frequency clock may be driven into XTL1IN or XTL2IN. The correct clock source must be selected using the MCK bits. Manipulating DFR bits will allow various divide ratios from the clock to be selected. SCLK and FSYNC must be synchronous to the external clock.

As a third alternative, SCLK may be programmed to be the master clock input. In this case, it must be 256 times Fs.

Serial Interface

The serial interface of the CS4215 transfers digital audio data and control data into and out of the device. Multiple CS4215 devices may share the same data lines. DSP's supported include the Motorola 56001 in network mode and a subset of the 'CHI' bus from AT&T/Intel.

Serial Interface Signals

Figure 7 shows an example of two CS4215 devices connected to a common controller. The Serial Data Out (SDOUT) and Serial Data In (SDIN) lines are time division multiplexed between the CS4215s.

The serial interface clock, SCLK, is used for transmitting and receiving data. SCLK can be generated by one of the CS4215s, or it can be input from an external SCLK source. When generated by an external source, SCLK must be synchronous to the master clock. Data is transmitted on the rising edge of SCLK and is received on the falling edge of SCLK. The SCLK frequency is always equal to the bit rate.

The Frame Synchronizing signal (FSYNC) is used to indicate the start of a frame. It may be output from one of the CS4215s, or it may be generated from an external controller. If FSYNC is generated externally, it must be high for at least 1 SCLK period, and it must fall at least 2 SCLKs before the start of a new frame (see Figure 8). It must also be synchronous to the master clock. The frequency of FSYNC is equal to the system sample rate (see Figure 8). Each CS4215 requires 64 SCLKs to transfer all the data. The SCLK frequency can be set to 64, 128, or 256 bits per frame, thereby allowing for 1, 2 or 4 CS4215s connected to the same bus.

In a typical multi-part scenario, one CS4215 (the master) would generate FSYNC and SCLK, while the other CS4215s (the slaves) would receive FSYNC and SCLK. The CLKOUT of the master would be connected to the CLKIN of each slave device as shown in Figure 7. Then, the master device would be programmed for the desired sample frequency (assuming one of the crystals is selected as the clock source), the number of bits per frame, and for SCLK and FSYNC to be outputs. The slave devices would be programmed to use CLKIN as the clock source, the same number of bits per frame, and for SCLK and FSYNC to be inputs. Since CLKOUT is al-

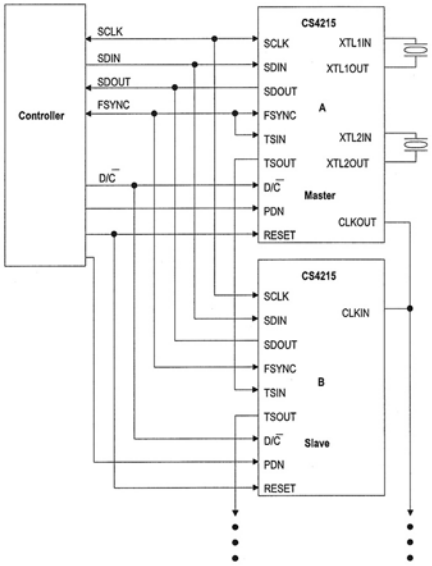


Figure 7. Multiple CS4215's

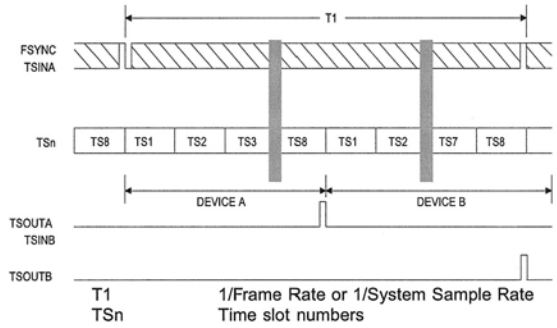


Figure 8. Serial Interface Timing for 2 CS4215's

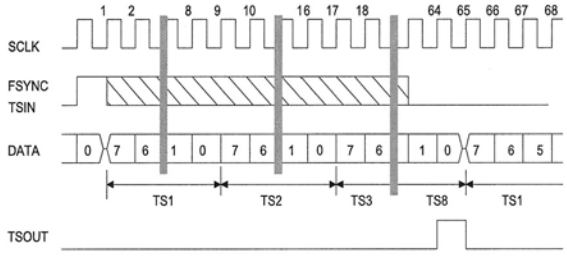


Figure 9. Frame Sync and Bit Offset Timing

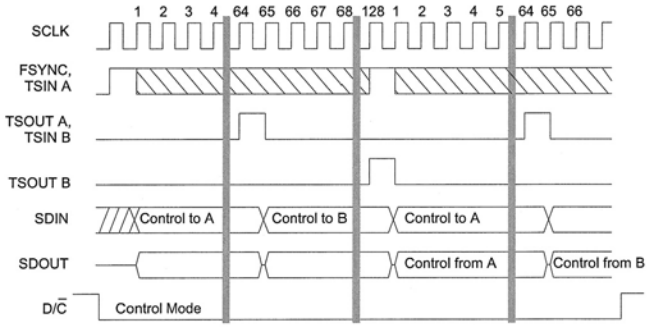


Figure 10. Control Mode Timing for 2 CS4215's

ways 256 times the sample frequency and scales with the selected sample frequency on the master, the slave devices will automatically scale with changes in the master codec's sample frequency.

CS4215s are time division multiplexed onto the bus using the Time Slot Out (TSOUT) and Time Slot In (TSIN) signals. TSOUT is an output signal that is high for one SCLK bit time, and indicates that the CS4215 is about to release the bus. TSIN is an input signal that informs the CS4215 that the next time slot is available for it to use. The first device in the chain uses FSYNC as its TSIN signal. All subsequent devices use the TSOUT of the previous device as its TSIN input. TSIN must be high for at least 1 SCLK period and fall at least 2 SCLKs before start of a new frame.

Serial Interface Operation

The serial interface format has a variable number of time slots, depending on the number of CS4215s attached to the bus. All time slots have 8 bits. Each CS4215 requires 8 time slots (64 bits) to communicate all data (see Figure 9).

CONTROL MODE

The Control Mode is used to set up the CS4215 for subsequent operation in Data Mode by loading the internal control registers. Control mode is asserted by bringing D/$\overline{C}$ low. If D/$\overline{C}$ is low during power up, then the CS4215 will enter control mode immediately. The SCLK and FSYNC pins are tri-stated, and the CS4215 will receive SCLK and FSYNC from an external source. If the CS4215 is in master mode (SCLK and FSYNC are outputs) and D/$\overline{C}$ is brought low, then SCLK & FSYNC will continue to be driven for a minimum of 4 and a maximum of 12 SCLKs, if the ITS bit = 0. If ITS is 1, SCLK and FSYNC will three-state immediately after D/$\overline{C}$ goes low. If D/$\overline{C}$ is brought low when the codec is programmed as master with ITS=0, the codec will timeout and release FSYNC and SCLK within 100µs. The values in the control registers for control of the serial ports are ignored in control mode. The data received on SDIN is stored into the control registers which have addresses matching their time slots. The data in the registers is transmitted on SDOUT with the time slot equal to the register number (see Figure 10).

The steps involved when going from data mode to control mode and back are shown in the flow chart in Figure 11.

Control Formats

The CS4215 control registers have the functions and time slot assignments shown in Table 1. The register address is the time slot number when D/$\overline{C}$ is 0. Reserved bits should be written as 0 and could be read back as 0 or 1. When comparing data read back, reserved bits should be masked. The SDOUT pin goes into a high-impedance state prior to Time Slot 1 and after Time Slot 8. The data listed below the register is its reset state.

The parallel port register is used to read and write the two open-drain input/output pins. The outputs are all set to 1 on RESET. PIO bits are read only in control mode. Note that, since PIO signals are open drain signals, an external device

Time slot	Description
1	Status
2	Data Format
3	Serial Port Control
4	Test
5	Parallel Port
6	RESERVED
7	Revision
8	RESERVED

Table 1. Control Registers

may drive them low even when they have been programmed as highs. Therefore, the value read back may differ from the value written. In the data mode, (D/$\overline{C}$=1), this register can be read and written to through the serial port as part of the Input Settings Registers. In control mode, (D/$\overline{C}$=0) these bits can only be read.

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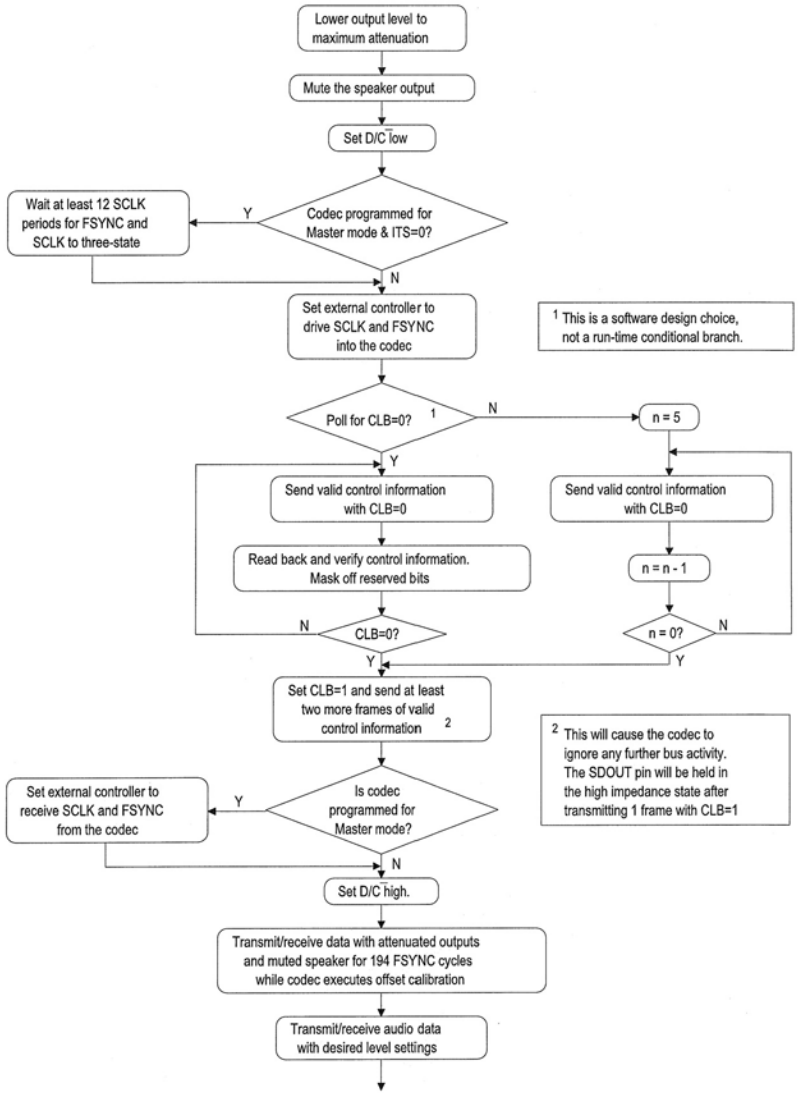

Figure 11. Control Mode Flow Chart