3. Dossier Annexes et Documentations Constructeurs

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La commande numérique accepte et interprète le code normalisé ISO :

Fonctions préparatoires :

G0	Déplacement rectiligne à grande vitesse
G1	Déplacement rectiligne à vitesse programmée
G2	Arc sens anti-trigonométrique à vitesse programmée
G3	Arc sens trigonométrique à vitesse programmée
G4	Temporisation

La précision du déplacement est prioritaire sur la vitesse d'usinage : la machine doit gérer les pentes d'accélération et de décélération pour respecter les cotes du déplacement.

Fonctions M de base

M0	Arrêt programmé
M2	Fin de programme

Fonctions M pour fraisage

M3	Démarrage broche
M5	Arrêt broche
M50	Montée patin aspiration copeaux
M51	Descente patin aspiration copeaux
M200	Démarrage aspiration plateau
M201	Arrêt aspiration plateau
M202	Démarrage aspiration copeaux
M203	Arrêt aspiration copeaux

Fonctions M pour laser

M3	Ouverture obturateur et démarrage aspiration fumées
M5	Fermeture obturateur et arrêt aspiration fumées
M20	Programmation puissance laser en usinage
M21	Programmation puissance laser à l'arrêt
M200	Démarrage aspiration fumées
M201	Arrêt aspiration fumées

Adresses :

X	Coordonnée en absolu axe X (mm)
Y	Coordonnée en absolu axe Y (mm)
Z	Coordonnée en absolu axe Z (mm)
I	Coordonnée en absolu du centre d'un arc de cercle en X
J	Coordonnée en absolu du centre d'un arc de cercle en Y
R	Rayon d'un arc de cercle
F	Vitesse d'avance (mm/mn) ou valeur temporisation (G4)
S	Vitesse de rotation de la broche (tr/mn) ou puissance laser en mW
T	Changement d'outil ou sélection programme laser (PP)

Autres

% n°	Numéro de programme
$ xxx	Insertion de commentaires

A.1 : Exemple de programme ISO pour CN5000 fraisage

```
%1                              En entête de tout programme
T1                              Sélection de l'outil
S30000 M3                       Démarrage de la broche à 30000 t/mn
G0 X109.374Y97.13
Z0.2
G1Z-10F1000                     Plongée de 10 mm à une vitesse de  1000 mm/mn
X90.626F3000                    Avance vers la position X=90.62mm à 3000mm/mn
Y102.87                         Avance vers la position 102.87 à 3000 mm/mn
.
.
X137.374
Y73.13
G2X133.374Y69.13I133.374J73.13
G1X66.626
.
.
G0Z10
X0Y0
M5                              Arrêt de la broche
M2                              Fin de programme
```

DGS 60, DGS 65 et DGS 66: Codeurs incrémentaux pour conditions ambiantes sévères.

FICHE PRODUIT

Nombre d'impulsions
100 à 10.000
Codeur incrémental

Sont disponibles des résolutions pouvant aller jusqu'à 10.000 impulsions/tour.
Vous pouvez composer vous-même votre propre codeur.
Variantes possibles arbre saillant 6 et 10 mm avec bride synchro ou de serrage arbre creux traversant ou non-traversant, avec sortie connecteur ou câble, interface TTL ou HTL.
Cette diversité de produits offre de nombreuses possibilités d'utilisation notamment sur des

- machines-outils
- machines textiles
- machines d'usinage du bois
- machines d'emballage

Les codeurs incrémentaux des gammes de construction DGS 60, DGS 65 et DGS 66 sont en service dans le monde entier dans les conditions ambiantes les plus sévères. Les caractéristiques remarquables de cette gamme de produits sont: une exécution robuste – le degré de protection pouvant aller jusqu'à IP 67– et la possibilité pour l'utilisateur d'adapter la forme de la construction à ses propres exigences.

SICK|STEGMANN

Codeur incrémental DGS 60, bride synchro/bride de serrage

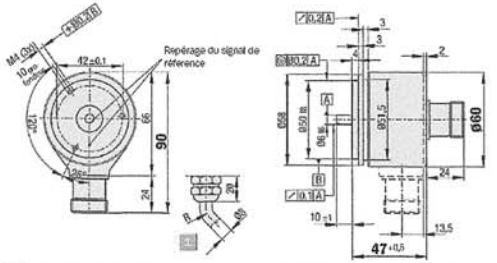
Nombre d'impulsions
100 à 10.000
Codeur incrémental

- Bride synchro/bride de serrage
- Sorties connecteur ou câble
- Degré de protection jusqu'à IP 67
- Interface électrique TTL et HTL

CE

Accessories
Raccordement électrique
Principe de fixation

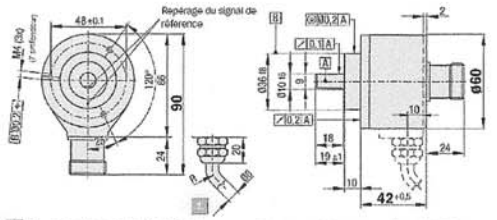
Plan technique bride synchro



R = rayon de courbure min. 40 mm

Tolérances générales selon DIN ISO 2768-mk

Plan technique bride de serrage



R = rayon de courbure min. 40 mm

Tolérances générales selon DIN ISO 2768-mk

Répartition des bornes et des fils

Borne	Signal pour HTL	Signal pour TTL	Couleur des fils (sortie câble)	Explication
1	N.C.	$\overline{B}$	noir	Liaison signal
2	N.C.	Sense +	gris	Raccordé à Us en interne
3	Z	Z	violet	Liaison signal
4	N.C.	$\overline{Z}$	jaune	Liaison signal
5	A	A	blanc	Liaison signal
6	N.C.	$\overline{A}$	brun	Liaison signal
7	N.C.	N.C.	orange	N.C.
8	B	B	rose	Liaison signal
9	Blindage	Blindage	Blindage	Potentiel du boîtier
10	GND	GND	bleu	Connection à la masse
11	N.C.	Sense –	vert	Raccordé à GND en interne
12	Us	Us	rouge	Tension d'alimentation*

Vue sur l'embase connecteur M23 du codeur

* Hors potentiel jusqu'au boîtier

N.C. = Non Connecté

Tournez la page S.V.P.

Codeur incrémental DGS 60, bride synchro/bride de serrage

Nombre d'impulsions
100 à 10.000

Codeur incrémental

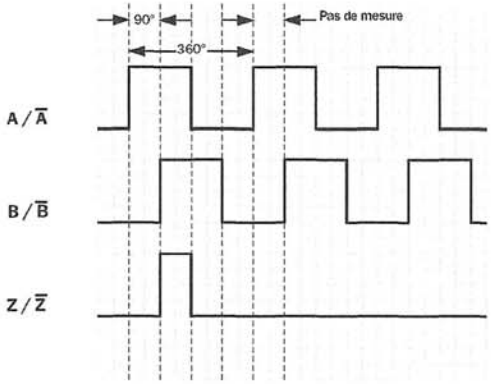
- Bride synchro/bride de serrage
- Sorties connecteur ou câble
- Degré de protection jusqu'à IP 67
- Interface électrique TTL et HTL

CE

Accessoires

Raccordement électrique
Principe de fixation

Sorties de signaux

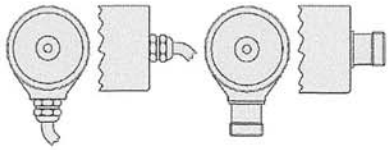


Interface électrique

Tension d'alimentation	4...6 V	10...30 V	10...30 V
Sortie	TTL (RS 422)	TTL (RS 422)	HTL (push-pull)

Type de connexion

Câble radial	Câble axial	Connecteur radial	Connecteur axial



DGS 60

Caractéristiques techniques	DGS 60	Type de bride: synchro	serrage
Arbre saillant	10 mm		
	6 mm		
Nombre d'impulsions (Z)par tour	00100 à 10.000 voir infos commande		
Attention nombre d'impulsions > 5000	uniquement avec TTL 4...6V		
Interfaces électriques	TTL / RS 422, 6 canaux		
	HTL / push-pull, 3 canaux (A, B, Z)		
Masse [1]	env. 0,3 kg		
Moment d'inertie du rotor			
Bride synchro	13 gcm²		
Bride de serrage	25 gcm²		
Pas de mesure	90° / nombre d'impulsions		
Signal de référence			
Nombre	1		
Largeur	90° électr. liaison logique avec A et B		
Limites d'erreurs			
100 ≤ Z < 1250	45 / Z + 0,054°		
1250 < Z ≤ 10000	45 / Z + 0,039°		
Déport du pas de mesure	45 / Z degrés		
Fréquence de sortie max.			
TTL	300 kHz (600 au-delà de 5000 impulsions)		
HTL	200 kHz		
Vitesse nominale max. [2]			
avec bague d'étanchéité à l'arbre	6.000 min⁻¹		
sans bague d'étanchéité à l'arbre	10000 min⁻¹		
Accélération angulaire max.	5 x 10⁵ rad/s²		
Couple résistant nominal			
avec bague d'étanchéité à l'arbre	1 Ncm		
sans bague d'étanchéité à l'arbre	0,1 Ncm		
Couple de démarrage			
avec bague d'étanchéité à l'arbre	1,5 Ncm		
sans bague d'étanchéité à l'arbre	0,2 Ncm		
Charge admissible à l'arbre			
Bride synchro radiale / axiale	20 N / 10 N		
Bride de serrage radiale / axiale	40 N / 20 N		
Durée de vie des roulements	3,6 x 10¹⁰ tours		
Plage de température de travail	- 20° ... + 85° C		
Plage de température de stockage	- 30° ... + 85° C		
Humidité relative de l'air tolérée [3]	90 %		
CEM [4]			
Tenue			
aux chocs [5]	30 / 11 g/ms		
aux vibrations [6]	20 / 10 ... 150 g/Hz		
Degré de protection selon IEC 60529 [7]			
Côté boîtier	IP 67		
Côté bride	IP 65		
Plage de tension d'alimentation			
Courant de TTL / RS 422, 4...6V	max. 20 mA		
sortie sous TTL / RS 422, 10...30V	max. 20 mA		
charge HTL / push-pull	max. 60 mA		
Consommation sans charge			
pour 24 V	100 mA		
pour 5 V	120 mA		

[1] Concerne produits avec sortie connecteur

[2] Pour un nombre de tours > 6000 RPM la bague d'étanchéité doit être retirée

[3] Condensation sur le module optique non tolérée

[4] Selon DIN EN 61000-6-4 et DIN EN 61000-6-1

[5] Selon DIN IEC 68 parties 2-27

[6] Selon DIN IEC 68 parties 2-6

[7] Avec contre-connecteur monté

Indications à la commande

Codeur incrémental DGS 60, arbre saillant

position 1	position 2	position 3	position 4	position 5	position 6	position 7	position 8	position 9	position 10	position 11	position 12	position 13	position 14
D	G	S	6	0	–								

Interfaces électriques

4...6 V, TTL (RS 422)	= A
10...30 V, TTL (RS 422)	= C
10...30 V, HTL (push-pull)	= G

Exécution méchanique

Bride synchro, arbre 6 mm	= 1
Bride de serrage, arbre 10 mm	= 4

Type de connexion

Connecteur M23, 12 pôl., radial	= A
Connecteur M23, 12 pôl., axial	= B
Câble 11 fils, radial 1,5 m	= K
Câble 11 fils, radial 3 m	= L
Câble 11 fils, radial 5 m	= M
Câble 11 fils, axial 1,5 m	= R
Câble 11 fils, axial 3 m	= S
Câble 11 fils, axial 5 m	= T

Nombre d'impulsions

libellé en clair, toujours à 5 positions

Nombre d'impulsions (Z) par tour

00100	00250	00500	00720	01024	02000	04000	07200[1]
00125	00256	00512	00750	01200	02048	04096	08000[1]
00150	00300	00570	00800	01250	02500	04500	08192[1]
00160	00314	00600	00900	01500	03000	05000	09000[1]
00180	00360	00625	01000	01800	03600	08000[1]	10000[1]
00200	00400	00700					

[1] uniquement possible avec interface électrique 4...6V, TTL (RS 422) = A

Exemple de commande de codeur incrémental DGS 60

4...6 Volt, TTL; Bride synchro; Connecteur M23, 12 pôles, radial; Nombre d'impulsions: 360

position 1	position 2	position 3	position 4	position 5	position 6	position 7	position 8	position 9	position 10	position 11	position 12	position 13	position 14
D	G	S	6	0	–	A	1	A	0	0	3	6	0

Veuillez insérer ici vos données de commande personnelles

position 1	position 2	position 3	position 4	position 5	position 6	position 7	position 8	position 9	position 10	position 11	position 12	position 13	position 14
D	G	S	6	0	–								
D	G	S	6	0	–								
D	G	S	6	0	–								

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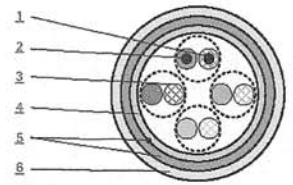
ACOLAN® - *cuivre*

Capillaires - FTP - 100 ohms - Catégorie 5e - 4P

Description

1 Diamètre du conducteur : 24AWG
2 Nature de l'isolant : Pe Ø < 1 mm
3 Assemblage : paires
Nombre de paires : 4
4 Ruban synthétique hydrofuge
5 Blindage général : ruban aluminium/polyester et fil de continuité
6 Type de gaine : LSOH ou PVC



Marquage de la gaine

ACOME 4P 24AWG FTP ENHANCED 100 OHMS M CAT5e
EC VERIFIED TO IS 11 801 IEC 332-1 75 C - N° de lot + métrique

Caractéristiques électriques à 20 °C

• Résistance linéique à 20 °C (max.)	98,6 Ω/km
• Rigidité diélectrique en courant continu 50Hz	1 kV/1min
• Résistance d'isolement (min.)	5 000 MΩ.km
• Déséquilibre de capacité réel-terre (max.)	800 pF/500 m
• Impédance de transfert (Zt) à 10 MHz (max.)	100 mΩ/m
• Vitesse de propagation (nom.)	78 %
• Impédance caractéristique (Zc) de 1 à 100 MHz	100 Ω

Caractéristiques environnementales

• Température de transport, stockage	0 °C + 50 °C
• Température de fonctionnement	-20 °C + 60 °C
• Tenue au feu	IEC 332-1, NFC 32070 2.1 (catégorie C2)

Caractéristiques mécaniques

Référence ACOME	Nombre de paires	Type de gaine (M)	Couleur de gaine	Ø du conducteur (mm)	Ø sur isolant (mm)	Ø du câble nominal (mm)	Poids du câble (kg/km)	Rayon de courbure min. à la pose (mm)	Tension max. de pose (N)
M4969	4P	LSOH	IVOIRE	0,51	0,98	5,90	38	50	80
M4967	4P	PVC	GRIS	0,51	0,98	5,90	37	50	80

Conditionnement

• 1 000 m sur touret KL ; 500 m sur touret KC ; 305 m sur ACOPACK

Fréquence (MHz)		1	4	10	16	20	31,25	62,5	100	155**	200**
Affaiblis. max. (dB/100 m)	Valeur typique	1,9	3,8	6	7,5	8,5	10,6	15,2	19,6	25	28
	Cat. 5e* (min.)	2,1	4,1	6,5	8,3	9,3	11,7	17	22	-	-
Min. Next (dB)	Valeur typique	72	63	57	54	52	49	45	42	39	37
	Cat. 5e* (min.)	65,3	56,3	50,3	47,3	45,8	42,9	38,4	35,3	-	-
Min. ACR (dB)	Valeur typique	70,1	59,2	51	46,5	43,5	38,4	29,8	22,5	14	9
	Cat. 5e* (min.)	63,2	52,2	43,8	39	36,5	31,2	21,4	13,3	-	-
PS Next (dB)	Valeur typique	69	60	54	51	49	46	42	39	36	34
	Cat. 5e* (min.)	62,3	53,3	47,3	44,3	42,8	39,9	35,4	32,3	-	-
ELFEXT (dB) (dB/100 m)	Valeur typique	75	63	55	51	48	45	39	35	31	29
	Cat. 5e* (min.)	64	52	44	40	38	34	28	24	-	-
PS ELFEXT (dB) (dB/100 m)	Valeur typique	72	60	52	48	45	42	36	32	28	26
	Cat. 5e* (min.)	61	49	41	37	35	31	25	21	-	-
Return Loss (dB)	Valeur typique	25	25	25	25	25	25	23,8	23	22	21
	Cat. 5e* (min.)	20	23	25	25	25	23,6	21,5	20,1	-	-

* Catégorie 5e selon DTR0366
** Pour information uniquement

Normes de références

Applications
• IEEE 802.3
• IEEE 802.5
• FDDI
• ATM
• RNIS

Normes câbles
• IEC 61 156-5
• EN 50 288-1 à -6

Normes système de câblages
• IS 11 801 ed.2
• EN 50 173
• EIA/TIA 568

Normes installation système de câblage
• EN 50 174

DIVISION TELECOM - 52, rue de Montparnasse - 75014 Paris - France - Tél. : +(33) 1 42 79 14 00 - Fax : +(33) 1 42 79 15 00
E-mail : DTLC@acome.fr - Site : www.acome.fr
Réf. DTLC 0772003 - 184 Fr

DSP56002

24-BIT DIGITAL SIGNAL PROCESSOR

The DSP56002 is a MPU-style general purpose Digital Signal Processor (DSP) composed of an efficient 24-bit DSP core, program and data memories, various peripherals, and support circuitry. The DSP56000 core is fed by on-chip Program RAM, and two independent data RAMs. The DSP56002 contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), parallel Host Interface (HI), Timer/Event Counter, Phase Lock Loop (PLL), and an On-Chip Emulation (OnCE™) port. This combination of features, illustrated in **Figure 1**, makes the DSP56002 a cost-effective, high-performance solution for high-precision general purpose digital signal processing.

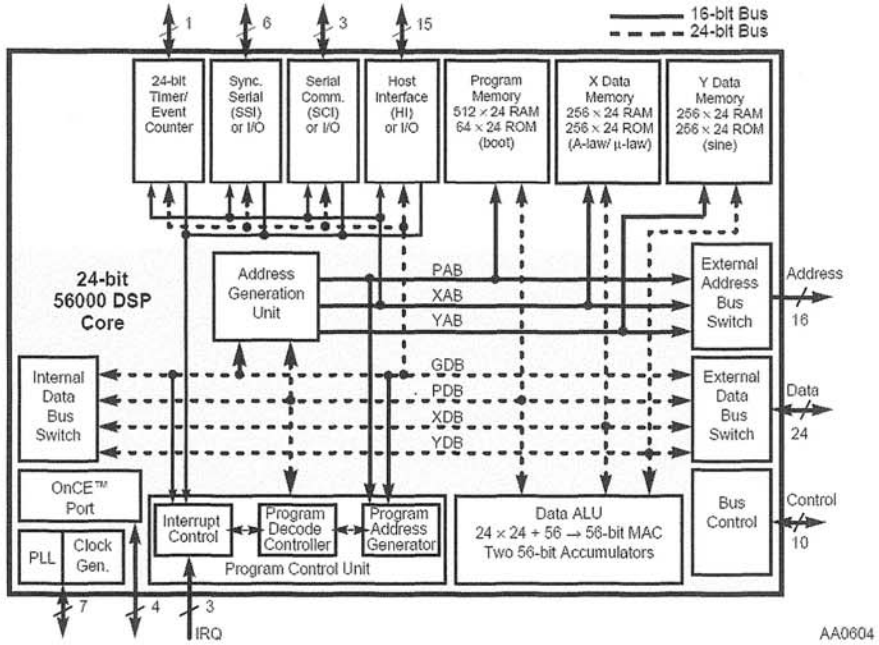


Figure 1 DSP56002 Block Diagram

FEATURES

Digital Signal Processing Core

- Efficient 24-bit DSP56000 core
- Up to 40 Million Instructions Per Second (MIPS), 25 ns instruction cycle at 80 MHz; up to 33 MIPS, 30.3 ns instruction cycle at 66 MHz
- Up to 240 Million Operations Per Second (MOPS) at 80 MHz; up to 198 MOPS at 66 MHz
- Performs a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
- Highly parallel instruction set with unique DSP addressing modes
- Two 56-bit accumulators including extension bits
- Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
- Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
- 56-bit addition/subtraction in 1 instruction cycle
- Fractional and integer arithmetic with support for multiprecision arithmetic
- Hardware support for block-floating point FFT
- Hardware nested DO loops
- Zero-overhead fast interrupts (2 instruction cycles)
- Four 24-bit internal data buses and three 16-bit internal address buses for maximum information transfer on-chip

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 512 × 24-bit on-chip Program RAM and 64 × 24-bit bootstrap ROM
- Two 256 × 24-bit on-chip data RAMs
- Two 256 × 24-bit on-chip data ROMs containing sine, A-law, and μ-law tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

SECTION 1

SIGNAL/PIN DESCRIPTIONS

INTRODUCTION

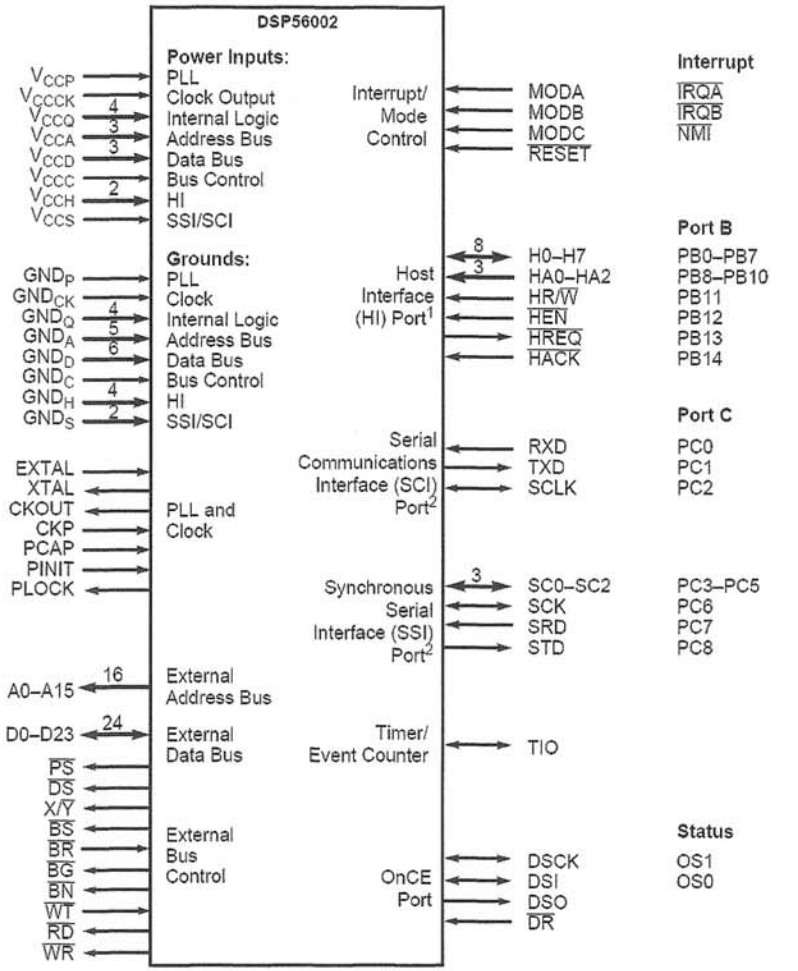
DSP56002 signals are organized into twelve functional groups, as summarized in Table 1-1.

Table 1-1 Signal Functional Group Allocations

Functional Group		Number of Signals	Detailed Description
Power (V_{CCX})		16	Table 1-2
Ground (GND_X)		24	Table 1-3
PLL and Clock		7	Table 1-4
Address Bus	Port A[1]	16	Table 1-5
Data Bus		24	Table 1-6
Bus Control		10	Table 1-7
Interrupt and Mode Control		4	Table 1-8
Host Interface (HI) Port	Port B[2]	15	Table 1-9
Serial Communications Interface (SCI) Port	Port C[3]	3	Table 1-10
Synchronous Serial Interface (SSI) Port		6	Table 1-11
Timer/Event Counter or General Purpose Input/Output (GPIO)		1	Table 1-12
On-Chip Emulation (OnCE) Port		4	Table 1-13

Note: 1. Port A signals define the External Memory Interface port.
2. Port B signals are the HI signals multiplexed on the external pins with the GPIO signals.
3. Port C signals are the SCI and SSI signals multiplexed on the external pins with the GPIO signals.

Figure 1-1 is a diagram of DSP56002 signals by functional group.



Note: 1. The Host Interface port signals are multiplexed with the Port B GPIO signals (PB0–PB15).
2. The SCI and SSI signals are multiplexed with the Port C GPIO signals (PC0–PC8).
3. Power and Ground lines are indicated for the 144-pin TQFP package.

AA1081G

Figure 1-1 Signals Identified by Functional Group

Tournez la page S.V.P.

ADDRESS BUS

Table 1-5 Address Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
A0–A15	Output	Tri-stated	**Address Bus**—These signals specify the address for external program and data memory accesses. If there is no external bus activity, A0–A15 remain at their previous values to reduce power consumption. A0–A15 are tri-stated when the bus grant signal is asserted.

DATA BUS

Table 1-6 Data Bus Signals

Signal Names	Signal Type	State during Reset	Signal Description
D0–D23	Input/ Output	Tri-stated	**Data Bus**—These signals provide the bidirectional data bus for external program and data memory accesses. D0–D23 are tri-stated when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.

BUS CONTROL

Table 1-7 Bus Control Signals

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{PS}$	Output	Tri-stated	**Program Memory Select**—$\overline{PS}$ is asserted low for external program memory access. $\overline{PS}$ is tri-stated when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.
$\overline{DS}$	Output	Tri-stated	**Data Memory Select**—$\overline{DS}$ is asserted low for external data memory access. $\overline{DS}$ is tri-stated when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.
X/$\overline{Y}$	Output	Tri-stated	**X/Y External Memory Select**—This output is driven low during external Y data memory accesses. It is also driven low during external exception vector fetches when operating in the Development mode. X/$\overline{Y}$ is tri-stated when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.
$\overline{BS}$	Output	Pulled high	**Bus Select**—$\overline{BS}$ is asserted when the DSP accesses the external bus, and it acts as an early indication of imminent external bus access by the DSP56002. It may also be used with the bus wait input $\overline{WT}$ to generate wait states. $\overline{BS}$ is pulled high when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.
$\overline{BR}$	Input	Input	**Bus Request**—When the Bus Request input ($\overline{BR}$) is asserted, it allows an external device, such as another processor or DMA controller, to become the master of the external address and data buses. While the bus is released, the DSP may continue internal operations using internal memory spaces. When $\overline{BR}$ is deasserted, the DSP56002 is the bus master.When $\overline{BR}$ is asserted, the DSP56002 will release Port A, including A0–A15, D0–D23, and the bus control signals ($\overline{PS}$, $\overline{DS}$, X/$\overline{Y}$, $\overline{RD}$, $\overline{WR}$, and $\overline{BS}$) by placing them in the high-impedance state after execution of the current instruction has been completed. Note: To prevent erroneous operation, pull up the $\overline{BR}$ signal when it is not in use.
$\overline{BG}$	Output	Pulled high	**Bus Grant**—When this output is asserted, it grants an external device's request for access to the external bus. This output is deasserted during hardware reset.

Table 1-7 Bus Control Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{BN}$	Output	Pulled low	**Bus Not Required**—The $\overline{BN}$ signal is asserted whenever the chip requires mastership of the external bus. During instruction cycles where the external bus is not required, $\overline{BN}$ is deasserted. If the $\overline{BN}$ signal is asserted when the DSP is not the bus master, processing has stopped and the chip is waiting to acquire bus ownership. An external arbiter may use this signal to help determine when to return bus ownership to the DSP. Note: The $\overline{BN}$ signal cannot be used as an early indication of imminent external bus access because it is valid later than the other bus control signals $\overline{BS}$ and $\overline{WT}$.
$\overline{WT}$	Input	Input	**Bus Wait**—An external device may insert wait states by asserting $\overline{WT}$ during external bus cycles. Note: To prevent erroneous operation, pull up the $\overline{WT}$ signal when it is not in use.
$\overline{WR}$	Output	Tri-stated	**Write Enable**—$\overline{WR}$ is asserted low during external memory write cycles. $\overline{WR}$ is tri-stated when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.
$\overline{RD}$	Output	Tri-stated	**Read Enable**—$\overline{RD}$ is asserted low during external memory read cycles. $\overline{RD}$ is tri-stated when the $\overline{BG}$ or $\overline{RESET}$ signal is asserted.

SERIAL COMMUNICATIONS INTERFACE PORT

Table 1-10 Serial Communications Interface (SCI+) Signals

Signal Name	Signal Type	State during Reset	Signal Description
RXD	Input	Tri-stated	**Receive Data (RXD)**—This input receives byte-oriented data and transfers the data to the SCI receive shift register. Input data can be sampled on either the positive edge or on the negative edge of the receive clock, depending on how the SCI control register is programmed.
PC0	Input or Output		**Port C GPIO 0 (PC0)**—This signal is a GPIO signal called PC0 when the SCI RXD function is not being used. After reset, the default state is GPIO input.
TXD	Output	Tri-stated	**Transmit Data (TXD)**—This output transmits serial data from the SCI transmit shift register. In the default configuration, the data changes on the positive clock edge and is valid on the negative clock edge. The user can reverse this clock polarity by programming the SCI control register appropriately.
PC1	Input or Output		**Port C GPIO 1 (PC1)**—This signal is a GPIO signal called PC1 when the SCI TXD function is not being used. After reset, the default state is GPIO input.
SCLK	Input or Output	Tri-stated	**SCI Clock (SCLK)**—This signal provides an input or output clock from which the receive or transmit baud rate is derived in the Asynchronous mode, and from which data is transferred in the Synchronous mode. The direction and function of the signal is defined by the RCM bit in the SCI+ Clock Control Register (SCCR).
PC2			**Port C GPIO 2 (PC2)**—This signal is a GPIO signal called PC2 when the SCI SCLK function is not being used. After reset, the default state is GPIO input.

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SYNCHRONOUS SERIAL INTERFACE PORT

Table 1-11 Synchronous Serial Interface (SSI) Signals

Signal Name	Signal Type	State during Reset	Signal Description
SC0 PC3	Input or Output	Tri-stated	**Serial Clock 0 (SC0)**—This signal's function is determined by whether the SCLK is in Synchronous or Asynchronous mode. • In Synchronous mode, this signal is used as a serial I/O flag. • In Asynchronous mode, this signal receives clock I/O. **Port C GPIO 3 (PC3)**—This signal is a GPIO signal called PC3 when the SSI SC0 function is not being used. After reset, the default state is GPIO input.
SC1 PC4	Input or Output	Tri-stated	**Serial Clock 1 (SC1)**—The SSI uses this bidirectional signal to control flag or frame synchronization. This signal's function is determined by whether the SCLK is in Synchronous or Asynchronous mode. • In Asynchronous mode, this signal is frame sync I/O. • For Synchronous mode with continuous clock, this signal is a serial I/O flag and operates like the SC0. SC0 and SC1 are independent serial I/O flags but may be used together for multiple serial device selection. **Port C GPIO 4 (PC4)**—This signal is a GPIO signal called PC4 when the SSI SC1 function is not being used. After reset, the default state is GPIO input.
SC2 PC5	Input or Output	Tri-stated	**Serial Clock 2 (SC2)**—The SSI uses this bidirectional signal to control frame synchronization only. As with SC0 and SC1, its function is defined by the SSI operating mode. **Port C GPIO 5 (PC5)**—This signal is a GPIO signal called PC5 when the SSI SC1 function is not being used. After reset, the default state is GPIO input.

Table 1-11 Synchronous Serial Interface (SSI) Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCK PC6	Input or Output	Tri-stated	**SSI Serial Receive Clock**—This bidirectional signal provides the serial bit rate clock for the SSI when only one clock is being used. **Port C GPIO 6 (PC6)**—This signal is a GPIO signal called PC6 when the SSI function is not being used. After reset, the default state is GPIO input.
SRD PC7	Input Input or Output	Tri-stated	**SSI Receive Data**—This input signal receives serial data and transfers the data to the SSI Receive Shift Register. **Port C GPIO 7 (PC7)**—This signal is a GPIO signal called PC7 when the SSI SRD function is not being used. After reset, the default state is GPIO input.
STD PC8	Output Input or Output	Tri-stated	**SSI Transmit Data (STD)**—This output signal transmits serial data from the SSI Transmitter Shift Register. **Port C GPIO 8 (PC8)**—This signal is a GPIO signal called PC8 when the SSI STD function is not being used. After reset, the default state is GPIO input.

HOST INTERFACE (HI) PORT

Table 1-9 HI Signals

Signal Name	Signal Type	State during Reset	Signal Description
H0–H7	Input or Output	Tri-stated	**Host Data Bus (H0–H7)**—This data bus transfers data between the host processor and the DSP56002. When configured as a Host Interface port, the H0–H7signals are tri-stated as long as $\overline{\text{HEN}}$ is deasserted. The signals are inputs unless HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, in which case H0–H7 become outputs, allowing the host processor to read the DSP56002 data. H0–H7 become outputs when $\overline{\text{HACK}}$ is asserted during $\overline{\text{HREQ}}$ assertion.
PB0–PB7			**Port B GPIO 0–7 (PB0–PB7)**—These signals are General Purpose I/O signals (PB0–PB7) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input.
HA0–HA2	Input	Tri-stated	**Host Address 0—Host Address 2 (HA0–HA2)**—These inputs provide the address selection for each Host Interface register.
PB8–PB10	Input or Output		**Port B GPIO 8–10 (PB8–PB10)**—These signals are General Purpose I/O signals (PB8–PB10) when the Host Interface is not selected. After reset, the default state for these signals is GPIO input.
HR/$\overline{\text{W}}$	Input	Tri-stated	**Host Read/Write**—This input selects the direction of data transfer for each host processor access. If HR/$\overline{\text{W}}$ is high and $\overline{\text{HEN}}$ is asserted, H0–H7 are outputs and DSP data is transferred to the host processor. If HR/$\overline{\text{W}}$ is low and $\overline{\text{HEN}}$ is asserted, H0–H7 are inputs and host data is transferred to the DSP. HR/$\overline{\text{W}}$ must be stable when $\overline{\text{HEN}}$ is asserted.
PB11	Input or Output		**Port B GPIO 11 (PB11)**—This signal is a General Purpose I/O signal called PB11 when the Host Interface is not being used. After reset, the default state for this signal is GPIO input.

Table 1-9 HI Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{\text{HEN}}$	Input	Tri-stated	**Host Enable**—This input enables a data transfer on the host data bus. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is high, H0–H7 become outputs and the host processor may read DSP56002/L002 data. When $\overline{\text{HEN}}$ is asserted and HR/$\overline{\text{W}}$ is low, H0–H7 become inputs. Host data is latched inside the DSP on the rising edge of $\overline{\text{HEN}}$. Normally, a chip select signal derived from host address decoding and an enable strobe are used to generate $\overline{\text{HEN}}$.
PB12	Input or Output		**Port B GPIO 12 (PB12)**—This signal is a General Purpose I/O signal called PB12 when the Host Interface is not being used. After reset, the default state for this signal is GPIO input.
$\overline{\text{HREQ}}$	Open drain Output	Tri-stated	**Host Request**—This signal is used by the Host Interface to request service from the host processor, DMA controller, or a simple external controller. Note: $\overline{\text{HREQ}}$ should always be pulled high when it is not in use.
PB13	Input or Output		**Port B GPIO 13 (PB13)**—This signal is a General Purpose (not open-drain) I/O signal (PB13) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input.
$\overline{\text{HACK}}$	Input	Tri-stated	**Host Acknowledge**—This input has two functions. It provides a host acknowledge handshake signal for DMA transfers and it receives a host interrupt acknowledge compatible with MC68000 family processors. Note: $\overline{\text{HACK}}$ should always be pulled high when it is not in use.
PB14	Input or Output		**Port B GPIO 14 (PB14)**—This signal is a General Purpose I/O signal (PB14) when the Host Interface is not selected. After reset, the default state for this signal is GPIO input.

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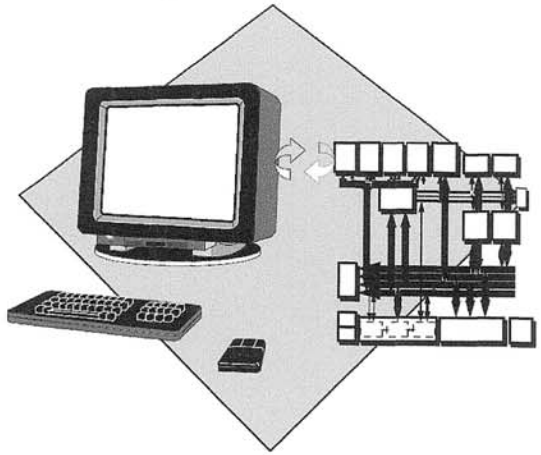
SERIAL HOST INTERFACE



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5.1 INTRODUCTION

The Serial Host Interface (SHI) is a serial I/O interface that provides a path for communication and program/coefficient data transfers between the DSP and an external host processor. The SHI can also communicate with other serial peripheral devices. The SHI can interface directly to either of two well-known and widely used synchronous serial buses: the Motorola Serial Peripheral Interface (SPI) bus and the Philips Inter-Integrated-circuit Control (I^2C) bus. The SHI supports either the SPI or I^2C bus protocol, as required, from a slave or a single-master device. To minimize DSP overhead, the SHI supports single-, double-, and triple-byte data transfers. The SHI has a 10-word receive FIFO that permits receiving up to 30 bytes before generating a receive interrupt, reducing the overhead for data reception.

When configured in the SPI mode, the SHI can:

- Identify its slave selection (in Slave mode)
- Simultaneously transmit (shift out) and receive (shift in) serial data
- Directly operate with 8-, 16- and 24-bit words
- Generate vectored interrupts, separately for receive and transmit events, and update status bits
- Generate a separate vectored interrupt in the event of a receive exception
- Generate a separate vectored interrupt in the event of a bus-error exception
- Generate the serial clock signal (in Master mode)

When configured in the I^2C mode, the SHI can:

- Detect/generate Start and Stop events
- Identify its slave (ID) address (in Slave mode)
- Identify the transfer direction (receive/transmit)
- Transfer data byte-wise according to the SCL clock line
- Generate ACK signal following a byte receive
- Inspect ACK signal following a byte transmit
- Directly operate with 8-, 16- and 24-bit words
- Generate vectored interrupts separately for receive and transmit events and update status bits
- Generate a separate vectored interrupt in the event of a receive exception
- Generate a separate vectored interrupt in the event of a bus error exception
- Generate the clock signal (in Master mode)

5.2 SERIAL HOST INTERFACE INTERNAL ARCHITECTURE

The DSP views the SHI as a memory-mapped peripheral in the X data memory space. The DSP may use the SHI as a normal memory-mapped peripheral using standard polling or interrupt programming techniques. Memory mapping allows DSP communication with the SHI registers to be accomplished using standard instructions and addressing modes. In addition, the MOVEP instruction allows interface-to-memory and memory-to-interface data transfers without going through an intermediate register. The single master configuration allows the DSP to directly connect to dumb peripheral devices. For that purpose, a programmable baud-rate generator is included to generate the clock signal for serial transfers. The host side invokes the SHI, for communication and data transfer with the DSP, through a shift register that may be accessed serially using either the I^2C or the SPI bus protocols. **Figure 5-1** shows the SHI block diagram.

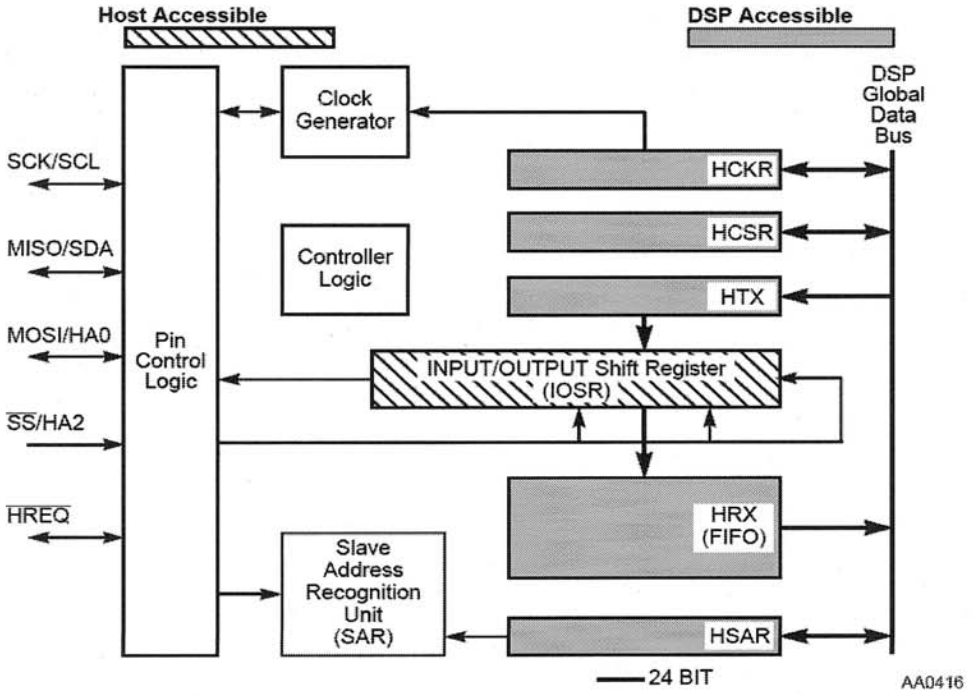

Figure 5-1 Serial Host Interface Block Diagram

5.2.1 SHI Clock Generator

The SHI clock generator generates the serial clock to the SHI if the interface operates in the Master mode. The clock generator is disabled if the interface operates in the Slave mode. When the SHI operates in the Slave mode, the clock is external and is input to the SHI (HMST = 0). **Figure 5-2** illustrates the internal clock path connections. It is the user's responsibility to select the proper clock rate within the range as defined in the I^2C and SPI bus specifications.

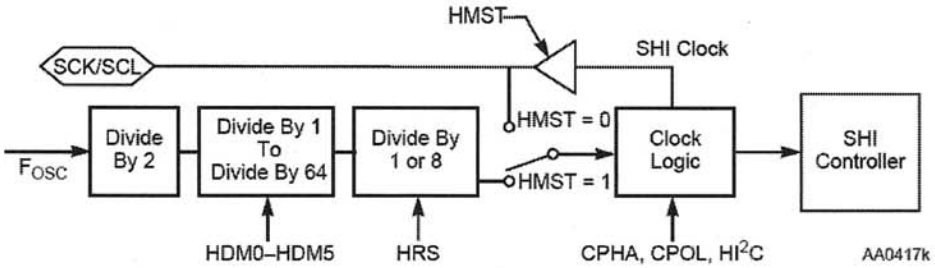

Figure 5-2 SHI Clock Generator

5.3 SERIAL HOST INTERFACE PROGRAMMING MODEL

The Serial Host Interface programming model is divided in two parts:

- **Host side**—see **Figure 5-3** below and **Section 5.3.1** on page 5-8
- **DSP side**—see **Figure 5-4** on page 5-6 and **Sections 5.3.2** on page 5-8 through **5.3.6** on page 5-14 for detailed information

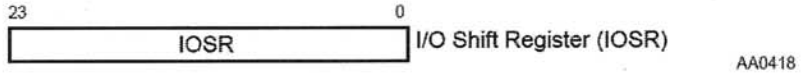

Figure 5-3 SHI Programming Model—Host Side

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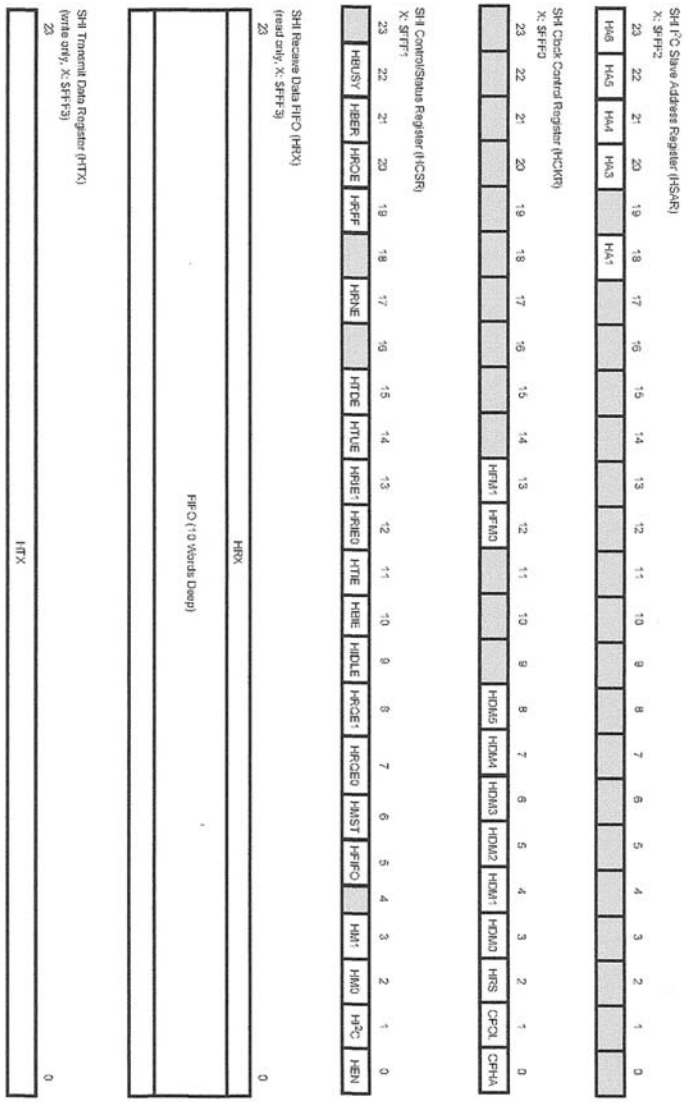
The interrupt vector table for the Serial Host Interface is shown in **Table 5-1** and the exceptions generated by the SHI are prioritized as shown in **Table 5-2** on page 5-7.

Table 5-1 SHI Interrupt Vectors

Address	Interrupt Source
P: $0020	SHI Transmit Data
P: $0022	SHI Transmit Underrun Error
P: $0024	SHI Receive FIFO Not Empty
P: $0026	Reserved
P: $0028	SHI Receive FIFO Full
P: $002A	SHI Receive Overrun Error
P: $002C	SHI Bus Error

Table 5-2 SHI Internal Interrupt Priorities

Priority	Interrupt
Highest	SHI Bus Error
	SHI Receive Overrun Error
	SHI Transmit Underrun Error
	SHI Receive FIFO Full
	SHI Transmit Data
Lowest	SHI Receive FIFO Not Empty



Reserved bit, read as 0, should be written with 0 for future compatibility

AA04190k

Figure 5-4 SHI Programming Model—DSP Side

5.3.1 SHI Input/Output Shift Register (IOSR)—Host Side

The variable length Input/Output Shift Register (IOSR) can be viewed as a serial-to-parallel and parallel-to-serial buffer in the SHI. The IOSR is involved with every data transfer in both directions (read and write). In compliance with the I^2C and SPI bus protocols, data is shifted in and out MSB first. In single-byte data transfer modes, the most significant byte of the IOSR is used as the shift register. In 16-bit data transfer modes, the two most significant bytes become the shift register. In 24-bit transfer modes, the shift register uses all three bytes of the IOSR (see **Figure 5-5**).

Note: The IOSR cannot be accessed directly either by the host processor or by the DSP. It is fully controlled by the SHI controller logic.

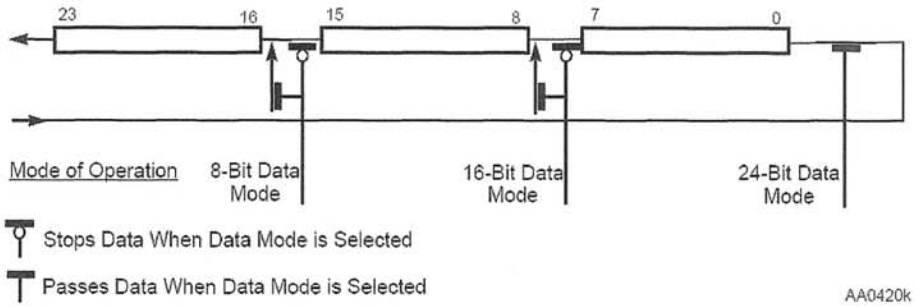


Figure 5-5 SHI I/O Shift Register (IOSR)

5.3.2 SHI Host Transmit Data Register (HTX)—DSP Side

The Host Transmit data register (HTX) is used for DSP-to-Host data transfers. The HTX register is 24 bits wide. Writing to the HTX register clears the HTDE flag. The DSP may program the HTIE bit to cause a Host transmit data interrupt when HTDE is set (see **5.3.6.10 HCSR Transmit-Interrupt Enable (HTIE)—Bit 11** on page 5-17). Data should not be written to the HTX until HTDE is set in order to prevent overwriting the previous data. HTX is reset to the empty state when in Stop mode and during hardware reset, software reset, and individual reset.

In the single-byte data transfer mode the most significant byte of the HTX is transmitted; in the double-byte mode the two most significant bytes, and in the triple-byte mode all the HTX is transferred.

5.3.3 SHI Host Receive Data FIFO (HRX)—DSP Side

The 24-bit Host Receive data FIFO (HRX) is a 10-word deep, First-In-First-Out (FIFO) register used for Host-to-DSP data transfers. The serial data is received via the shift register and then loaded into the HRX. In the single-byte data transfer mode, the most significant byte of the shift register is transferred to the HRX (the other bits are filled with 0s); in the double-byte mode the two most significant bytes are transferred (the least significant byte is filled with 0s), and in the triple-byte mode, all 24 bits are transferred to the HRX. The HRX may be read by the DSP while the FIFO is being loaded from the shift register. The HRX is reset to the empty state (cleared) when the chip is in Stop mode, and during hardware reset, software reset, and individual reset.

5.3.4 SHI Slave Address Register (HSAR)—DSP Side

The 24-bit Slave Address Register (HSAR) is used when the SHI operates in the I^2C Slave mode and is ignored in the other operational modes. HSAR holds five bits of the 7-bit slave address of the device. The SHI also acknowledges the general call address (all 0s, 7-bit address, and a 0 R/$\overline{W}$ bit) specified by the I^2C protocol. HSAR cannot be accessed by the host processor.

5.3.4.1 HSAR Reserved Bits—Bits 17–0,19

These bits are reserved and unused. They read as 0s and should be written with 0s for future compatibility.

5.3.4.2 HSAR I^2C Slave Address (HA[6:3], HA1)—Bits 23–20,18

Part of the I^2C slave device address is stored in the read/write HA[6:3], HA1 bits of HSAR. The full 7-bit slave device address is formed by combining the HA[6:3], HA1 bits with the HA0 and HA2 pins to obtain the HA[6:0] slave device address. The full 7-bit slave device address is compared to the received address byte whenever an I^2C master device initiates an I^2C bus transfer. During hardware reset or software reset, HA[6:3] = 1011 while HA1 is cleared; this results in a default slave device address of 1011_HA2_0_HA0.

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5.3.5 SHI Clock Control Register (HCKR)—DSP Side

The SHI Clock Control Register (HCKR) is a 24-bit read/write register that controls the SHI clock generator operation. The HCKR bits should be modified only while the SHI is in the individual reset state (HEN = 0 in the HCSR).

Note: The maximum-allowed internally generated bit clock frequency is $^{fosc}/_{4}$ for the SPI mode and $^{fosc}/_{6}$ for the I^2C mode (the maximum-allowed externally generated bit clock frequency is $^{fosc}/_{3}$ for the SPI mode and $^{fosc}/_{5}$ for the I^2C mode). The programmer should not use the combination HRS = 1 and HDM[5:0] = 000000, since it may cause synchronization problems and improper operation (it is therefore considered an illegal combination).

Note: The HCKR bits are cleared during hardware reset or software reset, except for CPHA, which is set. The HCKR is not affected by the Stop state.

The HCKR bits are described in the following paragraphs.

5.3.5.1 Clock Phase and Polarity (CPHA and CPOL)—Bits 1–0

The programmer may select any of four combinations of Serial Clock (SCK) phase and polarity when operating in the SPI mode (refer to **Figure 5-6** on page 5-11). The clock polarity is determined by the Clock Polarity (CPOL) control bit, which selects an active-high or active-low clock. When CPOL is cleared, it produces a steady-state low value at the SCK pin of the master device whenever data is not being transferred. If the CPOL bit is set, a high value is produced at the SCK pin of the master device whenever data is not being transferred.

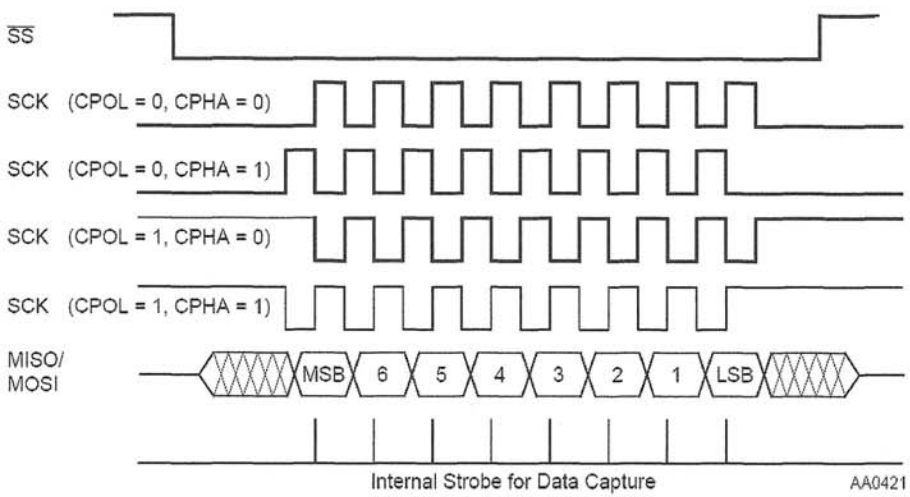

Figure 5-6 SPI Data-To-Clock Timing Diagram

The Clock Phase (CPHA) bit controls the relationship between the data on the MISO and MOSI pins and the clock produced or received at the SCK pin. This control bit is used in conjunction with the CPOL bit to select the desired clock-to-data relationship. The CPHA bit, in general, selects the clock edge that captures data and allows it to change states. It has its greatest impact on the first bit transmitted (MSB) in that it does or does not allow a clock transition before the data capture edge.

When in Slave mode and CPHA = 0, the $\overline{SS}$ line must be deasserted and asserted by the external master between each successive word transfer. $\overline{SS}$ must remain asserted between successive bytes within a word. The DSP core should write the next data word to HTX when HTDE = 1, clearing HTDE. However, the data will be transferred to the shift register for transmission only when $\overline{SS}$ is deasserted. HTDE is set when the data is transferred from HTX to the shift register.

When in Slave mode and CPHA = 1, the $\overline{SS}$ line may remain asserted between successive word transfers. The $\overline{SS}$ must remain asserted between successive bytes within a word. The DSP core should write the next data word to HTX when HTDE = 1, clearing HTDE. The HTX data will be transferred to the shift register for transmission as soon as the shift register is empty. HTDE is set when the data is transferred from HTX to the shift register.

When in Master mode and CPHA = 0, the DSP core should write the next data word to HTX when HTDE = 1, clearing HTDE; the data is transferred immediately to the shift register for transmission. HTDE is set only at the end of the data word transmission.

Note: The master is responsible for deasserting and asserting the slave device $\overline{SS}$ line between word transmissions.

When in Master mode and CPHA = 1, the DSP core should write the next data word to HTX when HTDE = 1, clearing HTDE. The HTX data will be transferred to the shift register for transmission as soon as the shift register is empty. HTDE is set when the data is transferred from HTX to the shift register.

The clock phase and polarity should be identical for both the master and slave SPI devices. CPHA and CPOL are functional only when the SHI operates in the SPI mode, and are ignored in the I^2C mode. The CPHA bit is set and the CPOL bit is cleared during hardware reset and software reset.

5.3.5.2 HCKR Prescaler Rate Select (HRS)—Bit 2

The HRS bit controls a prescaler in series with the clock generator divider. This bit is used to extend the range of the divider when slower clock rates are desired. When HRS is set, the prescaler is bypassed. When HRS is cleared, the fixed divide-by-eight prescaler is operational. HRS is ignored when the SHI operates in the Slave mode. The HRS bit is cleared during hardware reset and software reset.

5.3.5.3 HCKR Divider Modulus Select (HDM[5:0])—Bits 8–3

The HDM[5:0] bits specify the divide ratio of the clock generator divider. A divide ratio between 1 and 64 (HDM[5:0] = 0 to $3F) may be selected. When the SHI operates in the Slave mode, the HDM[5:0] bits are ignored. The HDM[5:0] bits are cleared during hardware reset and software reset.

5.3.5.4 HCKR Reserved Bits—Bits 23–14, 11–9

These bits in HCKR are reserved and unused. They are read as 0s and should be written with 0s for future compatibility.

5.3.5.5 HCKR Filter Mode (HFM[1:0]) — Bits 13–12

The read/write control bits HFM[1:0] specify the operational mode of the noise reduction filters as described in **Table 5-3** on page 5-13. The filters are designed to eliminate undesired spikes that might occur on the clock and data-in lines and allow the SHI to operate in noisy environments when required. One filter is located in the input path of the SCK/SCL line and the other is located in the input path of the data line (i.e., the SDA line when in I^2C mode, the MISO line when in SPI Master mode, and the MOSI line when in SPI Slave mode).

Table 5-3 SHI Noise Reduction Filter Mode

HFM1	HFM0	Description
0	0	Bypassed (Disabled)
0	1	Reserved
1	0	Narrow Spike Tolerance
1	1	Wide Spike Tolerance

When HFM[1:0] are cleared, the filter is bypassed (spikes are **not** filtered out). This mode is useful when higher bit-rate transfers are required and the SHI operates in a noise-free environment.

When HFM1 = 1 and HFM0 = 0, the narrow-spike-tolerance filter mode is selected. In this mode the filters eliminate spikes with durations of up to 20ns. This mode is suitable for use in mildly noisy environments and imposes some limitations on the maximum achievable bit-rate transfer.

When HFM1 = 1 and HFM0 = 1, the wide-spike-tolerance filter mode is selected. In this mode the filters eliminate spikes up to 100 ns. This mode is recommended for use in noisy environments; the bit-rate transfer is strictly limited. The wide-spike-tolerance filter mode is highly recommended for use in I^2C bus systems as it fully conforms to the I^2C bus specification and improves noise immunity.

Note: HFM[1:0] are cleared during hardware reset and software reset.

After changing the filter bits in the HCKR to a non-bypass mode (HFM[1:0] not equal to '00'), the programmer should wait at least ten times the tolerable spike width before enabling the SHI (setting the HEN bit in the HCSR). Similarly, after changing the I^2C bit in the HCSR or the CPOL bit in the HCKR, while the filter mode bits are in the non-bypass mode (HFM[1:0] not equal to '00'), the programmer should wait at least ten times the tolerable spike width before enabling the SHI (setting HEN in the HCSR).

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5.3.6 SHI Control/Status Register (HCSR)—DSP Side

The HCSR is a 24-bit read/write register that controls the SHI operation and reflects its status. Each bit is described in one of the following paragraphs. When in the Stop state or during individual reset, the HCSR status bits are reset to their hardware-reset state, while the control bits are not affected.

5.3.6.1 HCSR Host Enable (HEN)—Bit 0

The read/write control bit Host Enable (HEN) enables the overall operation of the SHI. When HEN is set, SHI operation is enabled. When HEN is cleared, the SHI is disabled (individual reset state, see below). The HCKR and the HCSR control bits are not affected when HEN is cleared. When operating in Master mode, HEN should be cleared only after the SHI is idle (HBUSY = 0). HEN is cleared during hardware reset and software reset.

5.3.6.1.1 SHI Individual Reset

While the SHI is in the individual reset state, SHI input pins are inhibited, output and bidirectional pins are disabled (high impedance), the HCSR status bits and the transmit/receive paths are reset to the same state produced by hardware reset or software reset. The individual reset state is entered following a one-instruction-cycle delay after clearing HEN.

5.3.6.2 HCSR I^2C/SPI Selection (HI^{2}C)—Bit 1

The read/write control bit HI^{2}C selects whether the SHI operates in the I^2C or SPI modes. When HI^{2}C is cleared, the SHI operates in the SPI mode. When HI^{2}C is set, the SHI operates in the I^2C mode. HI^{2}C affects the functionality of the SHI pins as described in **Section 2 Pin Descriptions**. It is recommended that an SHI individual reset be generated (HEN cleared) before changing HI^{2}C. HI^{2}C is cleared during hardware reset and software reset.

5.3.6.3 HCSR Serial Host Interface Mode (HM[1:0])—Bits 3–2

The read/write control bits HM[1:0] select the size of the data words to be transferred, as shown in **Table 5-4** on page 5-14. HM[1:0] should be modified only when the SHI is idle (HBUSY = 0). HM[1:0] are cleared during hardware reset and software reset.

Table 5-4 SHI Data Size

HM1	HMO	Description
0	0	8-bit data
0	1	16-bit data
1	0	24-bit data
1	1	Reserved

5.3.6.4 HCSR Reserved Bits—Bits 23, 18, 16, and 4

These bits in HCSR are reserved and unused. They are read as 0s and should be written with 0s for future compatibility.

5.3.6.5 HCSR FIFO-Enable Control (HFIFO)—Bit 5

The read/write control bit HCSR FIFO-enable control (HFIFO) selects the size of the receive FIFO. When HFIFO is cleared, the FIFO has a single level. When HFIFO is set, the FIFO has 10 levels. It is recommended that an SHI individual reset be generated (HEN cleared) before changing HFIFO. HFIFO is cleared during hardware reset and software reset.

5.3.6.6 HCSR Master Mode (HMST)—Bit 6

The read/write control bit HCSR Master (HMST) determines the operating mode of the SHI. If HMST is set, the interface operates in the Master mode. If HMST is cleared, the interface operates in the Slave mode. The SHI supports a single-master configuration, in both I^2C and SPI modes. When configured as an SPI Master, the SHI drives the SCK line and controls the direction of the data lines MOSI and MISO. The $\overline{SS}$ line must be held deasserted in the SPI Master mode; if the $\overline{SS}$ line is asserted when the SHI is in SPI Master mode, a bus error will be generated (the HCSR HBER bit will be set—see **Section 5.3.6.17 Host Bus Error (HBER)—Bit 21**). When configured as an I^2C Master, the SHI controls the I^2C bus by generating Start events, clock pulses, and Stop events for transmission and reception of serial data. It is recommended that an SHI individual reset be generated (HEN cleared) before changing HMST. HMST is cleared during hardware reset and software reset.

5.3.6.7 HCSR Host-Request Enable (HRQE[1:0])—Bits 8–7

The read/write Host-Request Enable control bits (HRQE[1:0]) are used to enable the operation of the $\overline{HREQ}$ pin. When HRQE[1:0] are cleared, the $\overline{HREQ}$ pin is disabled and held in the high impedance state. If either HRQE0 or HRQE1 are set and the SHI is operating in a Master mode, the $\overline{HREQ}$ pin becomes an input that controls SCK: deasserting $\overline{HREQ}$ will suspend SCK. If either HRQE0 or HRQE1 are set and the SHI is operating in a Slave mode, $\overline{HREQ}$ becomes an output and its operation is defined in **Table 5-5**. HRQE[1:0] should be modified only when the SHI is idle (HBUSY = 0). HRQE[1:0] are cleared during hardware reset and software reset.

Table 5-5 $\overline{\text{HREQ}}$ Function In SHI Slave Modes

HRQE1	HRQE0	$\overline{\text{HREQ}}$ Pin Operation
0	0	High impedance
0	1	Asserted if IOSR is ready to receive a new word
1	0	Asserted if IOSR is ready to transmit a new word
1	1	I^2C: Asserted if IOSR is ready to transmit or receive SPI: Asserted if IOSR is ready to transmit and receive

5.3.6.8 HCSR Idle (HIDLE)—Bit 9

The read/write control/status bit Host Idle (HIDLE) is used only in the I^2C Master mode; it is ignored otherwise. It is only possible to set the HIDLE bit during writes to the HCSR. HIDLE is cleared by writing to HTX. To ensure correct transmission of the slave device address byte, HIDLE should be set only when HTX is empty (HTDE = 1). After HIDLE is set, a write to HTX will clear HIDLE and cause the generation of a Stop event, a Start event, and then the transmission of the eight MSBs of the data as the slave device address byte. While HIDLE is cleared, data written to HTX will be transmitted 'as is.' If the SHI completes transmitting a word and there is no new data in HTX, the clock will be suspended after sampling ACK.

HIDLE determines the acknowledge that the receiver sends after correct reception of a byte. If HIDLE is cleared, the reception will be acknowledged by sending a '0' bit on the SDA line at the ACK clock tick. If HIDLE is set, the reception will not be acknowledged (a '1' bit is sent). It is used to signal an end-of-data to a slave transmitter by not generating an ACK on the last byte. As a result, the slave transmitter must release the SDA line to allow the master to generate the Stop event. If the SHI completes receiving a word and the HRX FIFO is full, the clock will be suspended before transmitting an ACK. While HIDLE is cleared the bus is busy, that is, the Start event was sent but no Stop event was generated. Setting HIDLE will cause a Stop event.

Note: HIDLE is set while the SHI is not in the I^2C Master mode. HIDLE is set during hardware reset, software reset, individual reset, and while the chip is in the Stop state.

5.3.6.9 HCSR Bus-Error Interrupt Enable (HBIE)—Bit 10

The read/write HCSR Bus-error Interrupt Enable (HBIE) control bit is used to enable the SHI bus-error interrupt. If HBIE is cleared, bus-error interrupts are disabled, and the HBER status bit must be polled to determine if an SHI bus error occurred. If both HBIE and HBER are set, the SHI will request SHI bus-error interrupt service from the interrupt controller. HBIE is cleared by hardware reset and software reset.

Note: Clearing HBIE will mask a pending bus-error interrupt only after a one-instruction-cycle delay. If HBIE is cleared in a long interrupt service routine, it is recommended that at least one other instruction separate the instruction that clears HBIE and the RTI instruction at the end of the interrupt service routine.

5.3.6.10 HCSR Transmit-Interrupt Enable (HTIE)—Bit 11

The read/write HCSR Transmit-Interrupt Enable (HTIE) control bit is used to enable the SHI transmit data interrupts. If HTIE is cleared, transmit interrupts are disabled, and the HTDE status bit must be polled to determine if the SHI transmit-data register is empty. If both HTIE and HTDE are set and HTUE is cleared, the SHI will request SHI transmit-data interrupt service from the interrupt controller. If both HTIE and HTUE are set, the SHI will request SHI transmit-underrun-error interrupt service from the interrupt controller. HTIE is cleared by hardware reset and software reset.

Note: Clearing HTIE will mask a pending transmit interrupt only after a one-instruction cycle-delay. If HTIE is cleared in a long interrupt service routine, it is recommended that at least one other instruction separate the instruction that clears HTIE and the RTI instruction at the end of the interrupt service routine.

5.3.6.11 HCSR Receive Interrupt Enable (HRIE[1:0])—Bits 13–12

The read/write HCSR Receive Interrupt Enable (HRIE[1:0]) control bits are used to enable the SHI receive-data interrupts. If HRIE[1:0] are cleared, receive interrupts are disabled, and the HRNE and HRFF (bits 17 and 19, see below) status bits must be polled to determine if there is data in the receive FIFO. If HRIE[1:0] are not cleared, receive interrupts will be generated according to **Table 5-6**.

Table 5-6 HCSR Receive Interrupt Enable Bits

HRIE[1:0]	Interrupt	Condition
00	Disabled	Not applicable
01	Receive FIFO not empty Receive Overrun Error	HRNE = 1 and HROE = 0 HROE = 1
10	Reserved	Not applicable
11	Receive FIFO full Receive Overrun Error	HRFF = 1 and HROE = 0 HROE = 1

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Note: HRIE[1:0] are cleared by hardware and software reset.

Note: Clearing HRIE[1:0] will mask a pending receive interrupt only after a one-instruction-cycle delay. If HRIE[1:0] are cleared in a long interrupt service routine, it is recommended that at least one other instruction separate the instruction that clears HRIE[1:0] and the RTI instruction at the end of the interrupt service routine.

5.3.6.12 HCSR Host Transmit Underrun Error (HTUE)—Bit 14

The read-only status bit Host Transmit Underrun Error (HTUE) indicates that a transmit-underrun error occurred. Transmit-underrun errors can occur only when operating in a Slave mode (in a Master mode, transmission takes place on demand and no underrun can occur). It is set when both the shift register and the HTX register are empty and the external master begins reading the next word:

- When operating in the I^2C mode, HTUE is set in the falling edge of the ACK bit. In this case, the SHI will retransmit the previously transmitted word.
- When operating in the SPI mode, HTUE is set at the first clock edge if CPHA = 1; it is set at the assertion of $\overline{SS}$ if CPHA = 0.

If a transmit interrupt occurs with HTUE set, the transmit-underrun interrupt vector will be generated. If a transmit interrupt occurs with HTUE cleared, the regular transmit-data interrupt vector will be generated. HTUE is cleared by reading the HCSR and then writing to the HTX register. HTUE is cleared by hardware reset, software reset, SHI individual reset, and during the Stop state.

5.3.6.13 HCSR Host Transmit Data Empty (HTDE)—Bit 15

The read-only status bit Host Transmit Data Empty (HTDE) indicates that the HTX register is empty and can be written by the DSP. HTDE is set when the data word is transferred from HTX to the shift register, except for a special case in SPI Master mode when CPHA = 0 (see HCKR). When operating in the SPI Master mode with CPHA = 0, HTDE is set after the end of the data word transmission. HTDE is cleared when HTX is written by the DSP. HTDE is set by hardware reset, software reset, SHI individual reset, and during the Stop state.

5.3.6.14 Host Receive FIFO Not Empty (HRNE)—Bit 17

The read-only status bit Host Receive FIFO Not Empty (HRNE) indicates that the Host Receive FIFO (HRX) contains at least one data word. HRNE is set when the FIFO is not empty. HRNE is cleared when HRX is read by the DSP, reducing the number of words in the FIFO to 0. HRNE is cleared during hardware reset, software reset, SHI individual reset, and during the Stop state.

5.3.6.15 Host Receive FIFO Full (HRFF)—Bit 19

The read-only status bit Host Receive FIFO Full (HRFF) indicates that the Host Receive FIFO (HRX) is full. HRFF is set when the HRX FIFO is full. HRFF is cleared when HRX is read by the DSP and at least one place is available in the FIFO. HRFF is cleared by hardware reset, software reset, SHI individual reset, and during the Stop state.

5.3.6.16 Host Receive Overrun Error (HROE)—Bit 20

The read-only status bit Host Receive Overrun Error (HROE) indicates that a data-receive overrun error occurred. Receive-overrun errors can not occur when operating in the I^2C Master mode, since the clock is suspended if the receive FIFO is full. HROE is set when the shift register (IOSR) is filled and ready to transfer the data word to the HRX FIFO and the FIFO is already full (HRFF is set). When a receive-overrun error occurs, the shift register is not transferred to the FIFO. If a receive interrupt occurs with HROE set, the receive-overrun interrupt vector will be generated. If a receive interrupt occurs with HROE cleared, the regular receive-data interrupt vector will be generated. HROE is cleared by reading the HCSR with HROE set, followed by reading HRX. HROE is cleared by hardware reset, software reset, SHI individual reset, and during the Stop state.

5.3.6.17 Host Bus Error (HBER)—Bit 21

The read-only status bit Host Bus Error (HBER) indicates that an SHI bus error occurred when operating as a master (HMST set). In I^2C mode, HBER is set if the transmitter does not receive an acknowledge after a byte is transferred; in this case, a Stop event will be generated and then transmission will be suspended. In SPI mode, the bit is set if $\overline{SS}$ is asserted; in this case, transmission is suspended at the end of transmission of the current word. HBER is cleared only by hardware reset, software reset, SHI individual reset, and during the Stop state.

5.3.6.18 HCSR Host Busy (HBUSY)—Bit 22

The read-only status bit Host Busy (HBUSY) indicates that the I^2C bus is busy (when in the I^2C mode) or that the SHI itself is busy (when in the SPI mode). When operating in the I^2C mode, HBUSY is set after the SHI detects a Start event and remains set until a Stop event is detected. When operating in the Slave SPI mode, HBUSY is set while $\overline{SS}$ is asserted. When operating in the Master SPI mode, HBUSY is set if the HTX register is not empty or if the IOSR is not empty. HBUSY is cleared otherwise. HBUSY is cleared by hardware reset, software reset, SHI individual reset, and during the Stop state.